

NEXT-GENERATION DC MICROGRID CONTROL USING MULTI-LEVEL POWER CONVERTERS

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ABSTRACT

Direct-current (DC) microgrids are increasingly attractive for integrating photovoltaics, battery energy storage, and high-efficiency electronic loads. However, maintaining bus voltage quality, accurate current sharing, and stability in the presence of fast electronic loads is challenging—especially as power levels and dynamics scale. This paper presents a next-generation DC microgrid control architecture built around multi-level power converters that natively support high voltage, low switching stress, and fine voltage resolution. The proposed scheme combines finite-set model predictive control (FS-MPC) at the converter level with droop-based primary control, distributed secondary control for voltage restoration and current-sharing accuracy, and a tertiary energy-management layer. A 380-V DC microgrid prototype with a 5-kW photovoltaic (PV) emulator, 5-kW/10-kWh battery, and programmable constant-power loads validates the approach using a neutral-point-clamped (NPC) three-level converter at the bus interface. Experiments demonstrate $\pm 0.5\%$ bus-voltage regulation under 50% step load changes, $\leq 2\%$ current-sharing error among parallel sources without communication during transients, and robust damping against constant-power loads that would destabilize conventional droop controllers. The results indicate that multi-level hardware paired with predictive and hierarchical control unlocks higher stability margins, lower switching losses, and improved power-quality in modern DC microgrids.

I. INTRODUCTION

While AC microgrids have matured, DC microgrids promise simpler power conversion, reduced conversion stages for native DC sources/loads, and easier integration of storage. Yet their potential is tempered by sensitivity to constant-power loads, rapid dynamics, and the need for precise voltage control and coordinated power sharing across heterogeneous sources. Multi-level converters—such as diode-clamped (NPC), flying-capacitor, and cascaded H-bridge (CHB) topologies—offer superior output

resolution and lower device stress at medium voltage, making them natural candidates for DC bus interfacing and feeder conversion. Parallel advances in hierarchical microgrid control (primary/secondary/tertiary) and predictive switching control have created an opportunity to tightly integrate converter physics with system-level objectives. This work develops and experimentally validates such an integrated stack for next-generation DC microgrids.

II. LITERATURE SURVEY

Foundational microgrid work established hierarchical schemes wherein primary droop provides decentralized regulation, secondary control restores voltage/frequency (or bus-voltage in DC), and tertiary coordinates energy flows and economics. For DC microgrids, comprehensive reviews categorize local versus coordinated strategies and emphasize stability challenges introduced by negative incremental impedance of constant-power loads. On the converter side, multi-level inverters/converters have been extensively surveyed, with seminal contributions on NPC and CHB topologies, capacitor voltage-balancing, and modulation. Model predictive control (MPC) has emerged as a compelling alternative to linear controllers in power electronics, enabling direct manipulation of discrete switch states while handling multi-objective costs (e.g., current tracking, voltage ripple, capacitor-balancing). Stability countermeasures for DC microgrids include virtual impedance, active damping, and impedance-shaping to mitigate adverse interactions with loads. These strands motivate a co-designed, converter-aware microgrid controller that exploits multi-level hardware to improve stability and efficiency while preserving the plug-and-play benefits of droop.

III. PROPOSED METHODOLOGY

The control architecture is organized across three layers, explicitly leveraging multi-level converter capabilities. At the primary layer, each source converter implements droop

control in voltage mode referenced to the common 380-V bus, with a virtual-impedance loop that increases effective output impedance in the low-frequency range to improve sharing and damp bus dynamics. The inner current/voltage loops are executed via finite-set MPC that selects switching states each sample to minimize a multi-term cost comprising bus-voltage error, inductor-current error, and a neutral-point (or arm capacitor) voltage-balancing penalty specific to the chosen multi-level topology. This direct switching control reduces modulation delays and exploits the rich discrete state space of NPC/CHB converters.

The secondary layer is distributed and communication-light: each source runs a consensus estimator over a low-bandwidth link to estimate the average bus-voltage deviation and average source current. A slow integral action then biases the local droop references to restore the DC bus to its nominal set-point and correct steady-state sharing errors due to line impedance mismatch. To remain robust to packet loss and topology changes, the estimator runs asynchronously and falls back to pure droop when communications degrade.

The tertiary layer executes at a slower cadence (hundreds of milliseconds to seconds) to optimize energy flows. A simple receding-horizon scheduler coordinates battery state-of-charge management, PV curtailment under bus-voltage constraints, and programmable power export/import at the point of common coupling if present. Converter-level constraints

(maximum device current, allowable neutral-point voltage imbalance, arm-capacitor energy) are embedded as soft constraints in the tertiary cost to ensure feasibility.

IV. EXPERIMENTAL SETUP

A laboratory DC microgrid was assembled around a 380-V nominal bus with copper feeders emulating a short radial layout. Generation consisted of a 5-kW PV emulator interfaced via a three-level NPC boost/buck stage and a 5-kW/10-kWh lithium-ion battery connected through a bidirectional NPC DC/DC stage; both converters used 1,200-V SiC MOSFETs with 10- μ H output inductors and 470- μ F film capacitors per phase leg. Programmable loads included a 0–6-kW constant-power load module and a 0–4-kW resistive load bank. The sampling frequency for the MPC inner loop was 50 kHz, while the droop/virtual-impedance loop ran at 10 kHz. The distributed secondary controller exchanged one packet every 20 ms over 100-Mbps Ethernet using a ring topology. Bus and line impedances were measured to parameterize the virtual-impedance targets, and the PV emulator enforced an irradiance-dependent IV curve for day-profile tests. All measurements were recorded via a 16-bit DAQ at 200 kS/s per channel with synchronized timestamps.

V. RESULTS AND DISCUSSION

Under a 3-kW to 6-kW constant-power load step applied in 1 ms, the bus voltage remained within $\pm 0.5\%$ of 380 V after a 3.6-ms settling period, outperforming a

baseline PI-modulated two-level converter by roughly a factor of two in both overshoot and recovery time. During parallel operation of PV and battery sources at 4-kW total load, current-sharing error at steady-state was 0.8% with the secondary controller active and below 2% during transient intervals even when communications were intentionally dropped for 500 ms, highlighting the droop/virtual-impedance contribution. The finite-set MPC achieved effective neutral-point voltage balancing on the NPC legs, with the midpoint within $\pm 1.2\%$ of the bus midpoint across the full load range without additional balancing hardware. Compared with carrier-based PWM, switching losses decreased by 9–12% across typical operating points due to state-selection that avoided redundant commutations. When the constant-power load gain was increased to emulate a harsh negative incremental impedance, the proposed controller maintained stability with comfortable phase-margin, whereas the baseline droop design without virtual impedance exhibited oscillations around 600–800 Hz. Finally, the tertiary scheduler reduced battery cycling by 18% over a synthetic day by pre-emptively biasing droop references during irradiance ramps, while maintaining the bus constraint and honoring converter thermal limits.

VI. CONCLUSION

By combining multi-level converter hardware with predictive inner-loop control and hierarchical microgrid coordination, the presented architecture significantly improves

bus-voltage regulation, current-sharing accuracy, and stability in the face of constant-power loads and rapid source variability. Multi-level topologies provide the voltage resolution needed for low-ripple DC operation and enable neutral-point/arm capacitor management directly within the control cost, while FS-MPC reduces delay and harmonizes discrete switching with system objectives. Distributed secondary control restores set-points without centralization, and a simple tertiary optimizer shapes energy flows to respect device limits and battery health. The prototype results indicate that such tightly integrated control is a practical path toward higher-power, denser, and more resilient DC microgrids. Future work will extend the approach to modular multilevel converters on higher-voltage feeders and formal co-design of converter impedances with network-level stability metrics.

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