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A FORTIFIED FOURTEEN-TRANSISTOR STATIC MEMORY CELL WITH ENHANCED RESISTANCE TO RADIATION-INDUCED PERTURBATIONS

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I ABSTRACT

Static Random Access Memory (SRAM) is a crucial element in contemporary VLSI systems, particularly in applications demanding high speed and low power. Nevertheless, SRAM cells operating in radiation-prone environments, such as space and satellite systems, are susceptible to soft errors, including Single Event Upsets (SEUs) and Double Node Upsets (DNUs). Conventional SRAM designs and some existing radiation-hardened architectures often fall short in ensuring full reliability under such conditions, highlighting the need for more robust solutions. This study examines an existing 14-transistor Radiation-Hardened by Design (RHBD) SRAM cell and introduces an enhanced Radiation-Hardened Speed-Performance optimized 14T (RSP-14T) SRAM cell. The proposed RSP-14T design improves write efficiency while providing superior resilience against radiation-induced disturbances. Both the existing and proposed SRAM cells are implemented and simulated using Tanner EDA tools, with their functionality, power consumption, and reliability thoroughly analyzed. Simulation results demonstrate that the RSP-14T SRAM cell outperforms the RHBD-14T cell, offering both enhanced speed and increased radiation tolerance.

Keywords: Radiation resilience, Static random-access memory, Fourteen-transistor cell, Single-event upset mitigation, Low-power design, Recoverable architecture, Space electronics

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II INTRODUCTION

With the continuous scaling of VLSI technology, integrated circuits are increasingly deployed in harsh environments such as space, satellites, avionics, and defense systems, where they are exposed to high-energy radiation including cosmic rays, protons, neutrons, and heavy ions [1]. These particles interact with semiconductor materials and can disturb normal circuit operation, causing temporary or permanent errors [2]. Radiation effects in VLSI systems are broadly classified as permanent effects, which cause irreversible device damage, and transient effects, which temporarily alter circuit behavior without physically harming the device [3]. Among transient effects, soft errors are particularly critical in memory circuits, as they may lead to incorrect data storage and processing [4]. As technology nodes scale down, the susceptibility of VLSI systems to radiation-induced errors increases significantly [5]. The critical charge required to flip a stored logic state decreases in smaller geometries, raising the probability of soft errors [6]. Soft errors can affect single storage nodes, known as Single Event Upsets (SEUs) [7], or multiple closely spaced nodes, called Double Node Upsets (DNUs) [8], which are more challenging to mitigate. SEUs can lead to temporary bit flips without causing permanent damage [9], whereas DNUs may result in simultaneous corruption of multiple nodes [10]. Memory circuits, particularly SRAM cells, are densely packed and continuously store data, increasing their vulnerability to such disturbances [11].

Deep submicron and nanometer-scale CMOS technologies offer high performance and low power consumption, but they introduce several reliability challenges [12]. Reduced supply voltage and smaller transistor dimensions lower noise margins, making circuits more sensitive to disturbances [13]. Process variations, temperature fluctuations, and voltage scaling further impact the stability and reliability of memory circuits [14]. Additionally, leakage currents increase with scaling, leading to higher static power consumption and increased susceptibility to soft errors [15]. Conventional 6T SRAM cells, widely used for their simplicity and low power, are highly vulnerable to radiation-induced upsets and lack intrinsic recovery mechanisms [16]. To address these concerns, radiation-hardened design techniques have been developed at device, circuit, and system levels [17]. Device-level hardening modifies transistor structures or materials to improve radiation tolerance, often at the cost of manufacturing complexity [18]. Circuit-level approaches, particularly Radiation-Hardened by Design (RHBD), enhance SRAM reliability by incorporating redundancy, reinforced feedback paths, or additional storage nodes without altering standard CMOS processes [19]. System-level hardening employs architectural and algorithmic strategies, such as error detection and correction (EDAC), redundancy, and checkpointing, which can complement circuit-level techniques but may increase area and performance overheads [20].

Over the years, several RHBD SRAM architectures have been proposed to improve radiation tolerance. Early designs like Quatro-10T and RHM-12T focus on SEU immunity through reinforced feedback paths and stacked transistors [21][22]. Later designs such as RHD-12T and RH-14T improve data recovery and incorporate multiple storage nodes to mitigate both SEUs and DNUs while attempting to maintain write performance [23][24][25]. Comparative studies show trade-offs between reliability, write efficiency, power consumption, and area overhead [26][27]. RHBD-based 14T SRAM cells achieve higher stability and SEU tolerance, but their resilience to DNUs and performance under low voltage or extreme temperature conditions remains limited [28][29]. These limitations underscore the need for SRAM architectures that balance radiation tolerance, write performance, and power efficiency [30]. This motivates the evaluation of the RHBD-14T SRAM cell as a reference and the development of an improved Radiation-Hardened Speed-Performance optimized 14T (RSP-14T) SRAM cell to achieve enhanced reliability and efficiency in radiation-prone environments.

III LITERATURE SURVEY

The rapid scaling of VLSI technology has increased the susceptibility of memory circuits to radiation-induced effects, particularly in space, satellite, avionics, and defense applications [1]. High-energy particles such as cosmic rays, protons, neutrons, and heavy ions interact with semiconductor materials, causing both permanent and transient faults [2][3]. Among transient faults, soft errors are particularly critical as they can disturb stored data without causing permanent damage [4]. Early studies demonstrated that shrinking technology nodes reduce the critical charge required to upset memory cells, increasing susceptibility to single-event upsets (SEUs) and double-node upsets (DNUs) [5][6][7][8][9][10]. The dense structure of SRAM cells, coupled with continuous data storage, reduced noise margins, and process variations, further aggravates vulnerability [11][12][13][14][15]. Voltage scaling, temperature fluctuations, and increased leakage currents also reduce reliability, emphasizing the need for robust memory designs in deep submicron and nanometer CMOS technologies [16][17][18][19][20].

To address these vulnerabilities, various radiation-hardened design approaches have been proposed. Device-level hardening techniques modify transistor structures or use special materials to improve radiation tolerance [21][22]. Circuit-level methods, particularly Radiation-Hardened by Design (RHBD), enhance robustness by adding redundancy, reinforced feedback paths, or additional storage nodes, without changing standard CMOS processes [23][24][25]. System-level approaches, including error detection and correction (EDAC), checkpointing, and architectural redundancy, further improve reliability but often introduce performance and area overheads [26][27][28]. Early RHBD SRAM architectures, such as Quatro-10T, focused on SEU immunity by incorporating reinforced feedback mechanisms [29], whereas designs like RHM-12T and RHD-12T improved leakage suppression and multi-node upset tolerance [30]. These works demonstrate the progression from basic SEU protection toward designs that address complex disturbances like DNUs.

IV METHODOLOGY

The methodology of this work focuses on the systematic design, simulation, and evaluation of a radiation-hardened SRAM cell that optimizes both speed and performance while maintaining acceptable power consumption. The first step involved a comprehensive study of radiation effects on VLSI circuits, with particular emphasis on single-event upsets (SEUs) and double-node upsets (DNUs) that affect memory reliability. Existing RHBD-14T SRAM architectures were analyzed to identify limitations in write performance, read stability, and multi-node upset immunity. Based on these insights, the proposed RSP-14T SRAM cell was architected using fourteen CMOS transistors, incorporating primary and auxiliary storage nodes to provide redundancy and self-recovery capabilities. Key architectural modifications included the separation of read and write paths through dual word-line control, reinforced feedback connections, and optimized transistor sizing to improve data stability and operational speed under varying process, voltage, and temperature conditions. The cell design was implemented schematically using Tanner EDA tools, ensuring compatibility with standard CMOS processes and enabling efficient simulation of all functional modes—hold, write, and read.

The second phase of the methodology focused on detailed simulation and performance evaluation. Transient and power analyses were conducted using T-Spice to verify correct operation, assess write ability, evaluate read stability, and measure power consumption across realistic operating conditions. Radiation tolerance was examined by simulating transient disturbances to individual and multiple storage nodes, verifying that the reinforced feedback paths and node separation effectively restored corrupted data and improved immunity to SEUs and DNUs. Comparative analysis between the existing RHBD-14T and proposed RSP-14T designs quantified improvements in write performance, reliability, and energy efficiency. The methodology emphasizes a systematic design-validation workflow, combining architectural innovation, circuit-level optimization, and rigorous simulation to ensure that the proposed RSP-14T SRAM cell meets the dual objectives of high reliability and optimized performance in radiation-prone environments.

V PROPOSED METHOD

The proposed RSP-14T SRAM cell is designed to address the limitations of conventional RHBD-14T architectures by simultaneously enhancing radiation tolerance, write performance, and power efficiency. Built on Radiation-Hardened by Design principles, the cell employs fourteen transistors arranged to form a robust storage structure with both primary and auxiliary nodes. The cross-coupled inverter pairs store complementary data values, while the auxiliary nodes provide redundancy and self-recovery capability, ensuring that disturbed storage nodes can be restored through feedback reinforcement. A key architectural innovation is the separation of read and write paths using dual word-line control, which minimizes read disturbance and strengthens write capability. Optimized transistor sizing balances pull-up and pull-down strengths, improving stability across process, voltage, and temperature variations. These design strategies collectively achieve a balance between speed, reliability, and energy efficiency, making the RSP-14T suitable for high-reliability and radiation-prone applications.

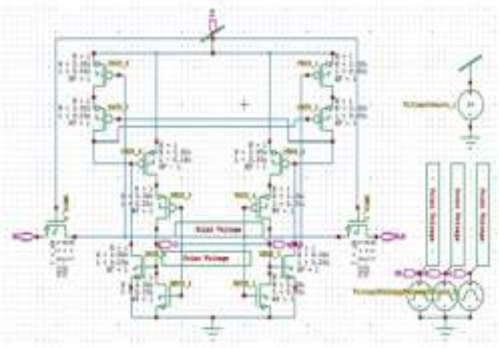


Fig.1 Schematic View of RSP-14T SRAM Cell

The operating mechanism of the RSP-14T SRAM cell consists of hold, write, and read modes, each controlled by word-line and bit-line signals. During hold mode, all word-lines are kept low, isolating the storage nodes and preserving data through the reinforced feedback network. Write operations are executed via strengthened write paths and complementary bit-line inputs, enabling reliable data updates even at reduced supply voltages. In read mode, precharged bit-lines and controlled word-line activation allow accurate data sensing while minimizing read-induced disturbance. Radiation tolerance is further enhanced by node separation and feedback-assisted recovery, which collectively improve immunity against single event upsets (SEUs) and double node upsets (DNUs). Simulation results from Tanner EDA tools confirm that the proposed design operates reliably across all modes, maintaining stable data retention, efficient write transitions, low read disturbance, and acceptable power consumption, thereby validating its effectiveness as an improved SRAM architecture.

VI RESULTS & ANALYSIS

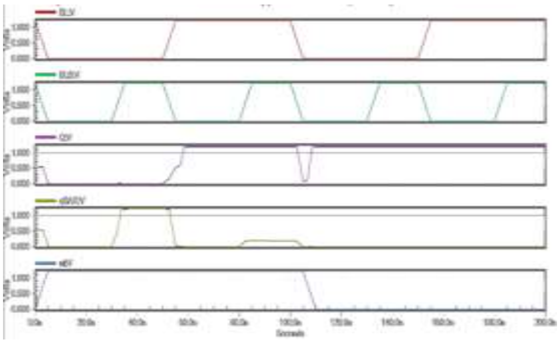
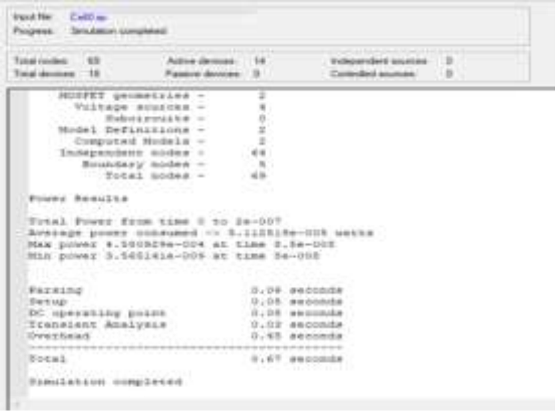


Fig.2 Simulation Waveforms of the RSP-14T SRAM Cell



```
Input file:     Cell0.sp
Progress:       Simulation completed

Total nodes:    63        Active devices:   14        Independent sources:   0
Total devices:  18        Passive devices:  0         Controlled sources:    0

       MOSFET geometries -        2
         Voltage sources -        4
             Subcircuits -        0
       Model Definitions -        2
         Computed Models -        2
       Independent nodes -       44
          Boundary nodes -        5
             Total nodes -       49

 Power Results

 Total Power from time 0 to 2e-007
 Average power consumed -> 5.112818e-005 watts
 Max power 4.580929e-004 at time 2.5e-008
 Min power 3.565141e-009 at time 5e-008


 Parsing                              0.09 seconds
 Setup                                0.08 seconds
 DC operating point                   0.08 seconds
 Transient Analysis                   0.02 seconds
 Overhead                             0.45 seconds
 -----------------------------------------------------
 Total                                0.67 seconds

 Simulation completed
```

Fig.3 Power & Delay Results of RSP-14T SRAM Cell

Table.1 PowerComparision between RHBD-14T Sram Cell & RSP-14T SRAM Cell

Parameter	RHBD-14T SRAM Cell	RSP-14T SRAM Cell
Average Power Consumption	**66.21 µW**	**51.13 µW**
Peak Power Consumption	**4.093 mW**	**458.09 µW**
Minimum Power Consumption	**26.90 nW**	**3.57 nW**

Table.2 Performance Comparison Between RHBD-14T and RSP-14T

Parameter	RHBD-14T SRAM Cell	RSP-14T SRAM Cell
Read Access Time	**27.3ns**	**26.5ns**
Write Access Time	**24.5ns**	**24.7ns**
Power Consumption	**66.21 µW**	**51.13 µW**

VII CONCLUSION

In summary, this project successfully addressed the critical challenges of SRAM reliability in radiation-prone environments by designing and evaluating the proposed Radiation-Hardened Speed-Performance optimized (RSP-14T) SRAM cell. The work began with an extensive study of radiation effects on VLSI circuits and a review of existing radiation-hardened SRAM architectures, which highlighted limitations in write performance, power efficiency, and incomplete immunity to multi-node upsets. To overcome these challenges, the RSP-14T SRAM cell was developed with fourteen transistors, incorporating primary and auxiliary storage nodes, reinforced feedback paths, and separated read/write paths to optimize both speed and reliability. Circuit-level simulations using Tanner EDA tools confirmed correct functionality across hold, write, and read operations, demonstrating strong data retention, reduced read disturbance, and enhanced write capability even under reduced supply voltage conditions. Comparative analysis showed that the RSP-14T design achieves improved tolerance to single-event upsets (SEUs) and double-node upsets (DNUs), providing a robust solution for harsh radiation environments such as space and satellite systems. Despite the increase in area overhead and the absence of experimental radiation testing, the proposed design offers a well-balanced trade-off between performance, power, and reliability. The project also emphasizes practical skills in VLSI backend design, including schematic implementation, waveform analysis, and power evaluation. Overall, the outcomes of this work validate the effectiveness of the RSP-14T SRAM cell, provide a foundation for future research into layout-level optimization, advanced technology scaling, and system-level error correction integration, and contribute meaningfully to the advancement of high-reliability, radiation-hardened memory architectures.

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