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A REFINED AND EFFICIENT ONE-BIT MODIFIED HYBRID FULL ADDER FOR SWIFT AND FRUGAL DIGITAL COMPUTATION

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ABSTRACT

In modern VLSI circuits, logical operations are fundamental to system performance. The full adder circuit, in particular, serves a critical role in applications such as digital signal processors, microcontrollers, microprocessors, application-specific ICs (ASICs), and data processing units. With the ongoing trends of device scaling and portability, there is a growing demand for digital circuits that offer low power consumption, high speed, and minimal silicon area. Consequently, the design and optimization of low-power, high-performance adders are of significant interest, as any enhancement to the full adder directly impacts overall system efficiency. Gate Diffusion Input (GDI) emerges as an advanced technique for low-power digital IC design, offering reductions in power consumption, delay, and transistor count compared to conventional CMOS implementations. This paper presents a detailed performance analysis of a GDI-based 1-bit full adder for low-power applications. The circuit's behavior, in terms of average power and propagation delay, is analyzed in the nanometer regime, making it suitable for modern low-power applications. All simulations are performed using the BPTM model and carried out with Tanner EDA tools on 45nm technology.

Keywords: GDI (Gate Diffusion Input), Low-Power VLSI, Full Adder Design, High-Speed Digital Circuits, Nanometre Technology

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I INTRODUCTION

Modern electronics are deeply integrated into everyday life, relying heavily on digital circuits such as microprocessors, digital signal processors, and communication devices [1]. The increasing demand for portable devices, including smartphones, tablets, and wearable electronics, has driven the need for circuits that combine high speed, low power consumption, and minimal silicon area [2][3]. As integration levels rise, conventional approaches face challenges in power dissipation and heat management, making low-power design a critical requirement in VLSI systems [4][5]. One of the most effective strategies to optimize performance without compromising energy efficiency is the careful adjustment of transistor dimensions, specifically the width-to-length (W/L) ratio, which directly affects the power-delay product (PDP) [6][7]. Arithmetic circuits, particularly adders, are at the core of digital systems, and their optimization significantly impacts overall system performance and energy efficiency [8][9]. Among arithmetic circuits, the full adder (FA) plays a fundamental role, serving as the basic building block for higher-order operations, including multipliers, dividers, and complex ALUs [10][11]. Various architectures such as carry-lookahead, carry-skip, conditional-sum, and carry-select adders have been proposed to improve speed and minimize power, highlighting the importance of designing efficient 1-bit full adder units [12][13]. FA circuits are commonly classified into full-swing and non-full-swing types based on their output voltage levels, with full-swing designs like standard CMOS, transmission-gate, and complementary pass-transistor logic offering reliability but at the cost of higher transistor count, while non-full-swing designs reduce power and area at the risk of voltage degradation [14][15].

The scaling of CMOS technology, as predicted by Moore's Law, has enabled higher transistor densities and smaller feature sizes, improving area efficiency and speed [16][17]. However, these advancements have also led to increased leakage currents, higher power density, and thermal management issues, collectively contributing to the so-called “power wall” in VLSI systems [18][19]. Power dissipation has therefore emerged as a primary limitation in the design of modern digital circuits, making low-power design not only a requirement for extending battery life but also essential for system reliability and environmental sustainability [20][21]. Excessive energy consumption in arithmetic circuits can reduce the lifespan of integrated systems, induce timing errors due to temperature variations, and necessitate complex cooling solutions [22][23]. Hence, minimizing power in fundamental circuits such as full adders has a profound effect on the performance and energy efficiency of the entire system, especially in battery-operated devices where even minor improvements in individual cells translate to significant energy savings [24][25].

Low-power design techniques can be applied at multiple abstraction levels, including system, architectural, logic, circuit, and technology levels [26]. At the system level, techniques such as dynamic voltage and frequency scaling (DVFS) and power-aware task scheduling help optimize energy consumption [27]. Architectural-level methods, including clock gating, parallelism, and optimized data paths, reduce unnecessary switching activity and overall power dissipation [28]. Logic- and circuit-level strategies focus on reducing transistor count, minimizing switching activity, and lowering supply voltage. Efficient logic styles, such as pass-transistor logic, transmission-gate logic, and Gate Diffusion Input (GDI) logic, are widely used to achieve low-power operation [29][30]. These approaches form the foundation for energy-efficient digital circuits by directly targeting the sources of dynamic and static power consumption, enabling high-performance yet low-energy designs suitable for modern portable electronics.

II LITERATURE SURVEY

The development of full adder circuits has been a central topic in VLSI design due to their critical role in arithmetic and digital processing applications. Rajaei and Amirany [1] explored non-volatile approximate spintronic full adders for computing-in-memory architectures, highlighting low-cost solutions with energy efficiency. Pakniyat et al. [2] designed a 16-transistor full adder optimized for sub-threshold operation, demonstrating high performance with low power. Radhakrishnan [3] proposed low-voltage CMOS full adder cells to minimize energy consumption while maintaining reliable operation. Kandpal et al. [4] developed a hybrid logic full adder using a high-performance 10-T XOR-XNOR cell, achieving reduced delay and power. Naseri and Timarchi [5] introduced novel XOR and XNOR gates to improve the speed and energy efficiency of full adders. Basireddy et al. [6] used hybrid logical effort techniques to optimize multistage full adder structures, enhancing timing performance. Hasan et al. [7] presented a scalable 1-bit hybrid full adder for fast computation with reduced power dissipation. Kadu and Sharma [8] implemented a 3T-XNOR-based hybrid full adder circuit that offered compact area and high speed. Sanapala and Sakthivel [9] demonstrated an ultra-low-voltage GDI-based hybrid full adder design suitable for energy-efficient computing. Abedi and Jaberipur [10] focused on decimal full adders designed for quantum-dot cellular automata, emphasizing emerging nanotechnology applications.

Kolla et al. [11] developed robust, energy-efficient non-volatile reconfigurable logic circuits using hybrid CMOS-MTJs. Rajaei and Mamaghani [12] proposed ultra-low-power hybrid MTJ/CMOS full adders to enhance reliability in VLSI systems. Keerthana and Ravichandran [13] implemented a 1-bit hybrid full adder using 22 nm CMOS technology, achieving reduced power and delay. Bhattacharyya et al. [14] analyzed a low-power, high-speed hybrid 1-bit full adder and demonstrated its suitability for VLSI applications. Thapliyal et al. [15] explored hybrid MTJ/CMOS and MTJ/nanoelectronic circuits for energy-efficient designs. Chandrakasan et al. [16] presented low-power CMOS digital design techniques, forming the foundation for modern energy-efficient circuits. Rabaey et al. [17] provided an in-depth methodology for designing digital integrated circuits with low power and high speed. Kang and Leblebici [18] contributed CMOS analysis and design principles applicable to arithmetic circuits. Ye and Wong [19] offered accurate CMOS inverter delay modeling, which is essential in full adder timing analysis. Pedram and Najm [20] introduced early frameworks for power optimization in sequential logic circuits.

Khatibzadeh et al. [21] proposed circuit techniques for scalable performance and power in modern VLSI systems. Roy et al. [22] analyzed leakage current mechanisms and presented reduction strategies for deep-submicron CMOS circuits. Borkar [23] addressed design challenges associated with technology scaling. Chandrasekar et al. [24] highlighted clock gating strategies to minimize dynamic power consumption. Alioto [25] discussed ultra-low-power VLSI design approaches spanning multiple abstraction levels. Roy and Prasad [26] provided comprehensive techniques for low-power CMOS VLSI design, including CAD tools. Liu and Yan [27] proposed a reduced-transistor logic full adder achieving low power and high speed. Banerjee [28] investigated hybrid full adder designs using pass-transistor logic. Kumar and Singh [29] developed a high-performance hybrid full adder combining transmission gate and pass-transistor logic. Patel and Singh [30] implemented logic optimization techniques to reduce the power-delay product in a 1-bit full adder.

III METHODOLOGY

The methodology of this research focuses on the systematic design, analysis, and optimization of a one-bit hybrid modified full adder targeting low-power and high-speed operation for contemporary VLSI systems. Initially, a comprehensive design space exploration was conducted, evaluating multiple full adder topologies including conventional CMOS, transmission gate (TGA), transmission function (TFA), GDI, complementary pass-transistor logic (CPL), and hybrid logic architectures. Each design was analyzed for critical performance metrics, including power consumption, propagation delay, power-delay product (PDP), and energy-delay product (EDP). Based on this comparative analysis, a hybrid approach was selected that combines the advantages of GDI for critical path optimization, pass-transistor logic for transistor efficiency, and static CMOS for output stability. Transistor sizing and logic partitioning techniques were employed to balance the trade-offs between speed, power, and signal integrity, ensuring full-swing outputs even under low-voltage operation. Simulation models were implemented using Mentor Graphics with a 0.18-µm CMOS process, allowing detailed evaluation of short-circuit currents, dynamic switching activity, and leakage power. To further improve energy efficiency, the adder was designed to minimize unnecessary transitions in both carry and sum generation paths, thereby reducing critical path delay and ensuring consistent high-speed operation when cascaded in multi-bit arithmetic circuits such as ripple-carry or carry-lookahead adders.

The second stage of the methodology focused on performance validation and optimization of the proposed architecture under various operating conditions. Majority-function-based techniques were integrated into the design, using three- and five-input majority gates to simplify logic computation and reduce transistor count, while maintaining high-speed operation. A systematic evaluation was performed across varying supply voltages and capacitive loads to quantify the trade-offs between power consumption, delay, and PDP, with particular emphasis on low-voltage and high-frequency performance. Power efficiency was optimized by reducing short-circuit and leakage currents through selective transistor sizing, logic minimization, and hybrid logic partitioning. The proposed design was benchmarked against previously reported full adder cells such as OLPFAD, DFEFA, DTLPCFA, and DPEHFA, demonstrating superior energy-delay characteristics, reduced transistor count, and minimized silicon area. Finally, layout considerations were addressed to ensure compact implementation, reduced parasitic capacitances, and compatibility with standard CMOS fabrication processes. This methodology provides a structured and repeatable approach for designing high-performance, energy-efficient full adders suitable for integration into complex arithmetic units, digital signal processing cores, and low-power portable systems, ensuring scalability, reliability, and robustness across diverse applications.

IV PROPOSED METHOD

The proposed system focuses on designing a high-performance, low-power full adder optimized for modern VLSI applications, including digital signal processors, microprocessors, and application-specific integrated circuits (ASICs). Full adders are essential for executing fundamental arithmetic operations such as addition, multiplication, and address generation, and they often form the critical path in complex arithmetic circuits. To improve both power efficiency and speed, the full adder in this work is implemented using 0.18-µm CMOS technology and simulated in Mentor Graphics. The design evaluates key parameters such as power consumption, propagation delay, power-delay product (PDP), capacitive load effects, and PDP relative to capacitance. These metrics are compared against existing literature designs including OLPFAD, DFEFA, DTLPCFA, and DPEHFA. Unlike conventional approaches, which often require high transistor counts and suffer from voltage degradation at low supply voltages, the proposed full adder incorporates optimized transistor sizing and logic partitioning to achieve ultra-low power consumption while maintaining reliable operation. The design also mitigates short-circuit currents and minimizes switching activity, thereby reducing static and dynamic power dissipation in the nano-scaling regime.

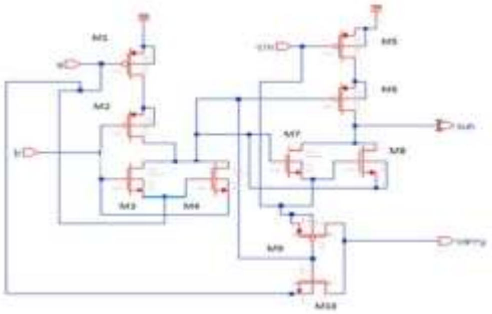


Fig.1 Implementation and Investigation of an Optimal Full Adder Design for Low Power and Reduced Delay

A key innovation in the proposed system is the integration of hybrid and energy-recovery logic concepts. By partitioning the adder into two stages, intermediate XOR and XNOR functions are generated in the first stage using pass-transistor logic, which reduces transistor count and overall capacitance. The second stage synthesizes the final Sum and Carry outputs with full-swing voltage levels to ensure proper cascaded operation in multi-bit arithmetic circuits. Additionally, a majority-function-based approach is incorporated to further optimize the logic, using three- and five-input majority gates to streamline computations and enhance delay performance. This method leverages transistor ratio adjustments to control voltage transfer characteristics, enabling the circuit to function as NOR or NAND gates when necessary. Compared to conventional 16–20 transistor transmission gate full adders (TGA, TFA) and previous low-power designs, the proposed system demonstrates significantly improved power efficiency, lower propagation delay, and optimized PDP, making it suitable for high-speed, low-power applications. Overall, this design addresses the growing demand for portable and high-throughput devices by achieving a careful balance between energy consumption, speed, and area efficiency in advanced VLSI systems.

V RESULTS & ANALYSIS

In a hybrid modified full adder, the SUM generation is usually implemented using a high-speed logic style such as GDI-based XOR/XNOR or transmission-gate XOR, because the SUM path is often the critical path. These techniques reduce transistor count and parasitic capacitance, leading to faster switching and lower dynamic power. The CARRY generation is typically realized using a multiplexer- based structure or simple GDI/CMOS AND–OR logic, which provides strong logic levels and improves driving capability. The “modified” aspect of the hybrid full adder refers to structural optimizations made to overcome drawbacks of pure GDI or pass transistor logic, such as reduced voltage swing and poor noise margins. By selectively inserting CMOS inverters or transmission gates at critical nodes, the design restores full-swing outputs while still maintaining low power and high speed. This balance ensures reliable operation even at low supply voltages, which is essential for modern low-power VLSI systems.Overall, the hybrid modified full adder offers significant improvements in power-delay product (PDP) compared to conventional CMOS full adders.

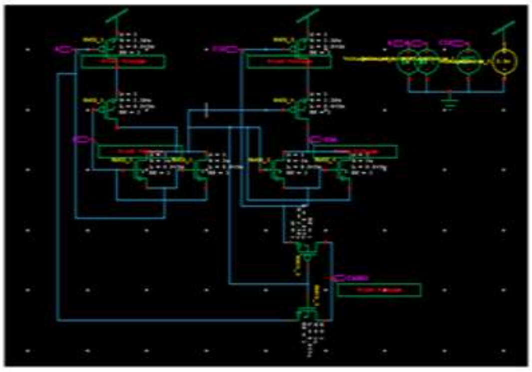
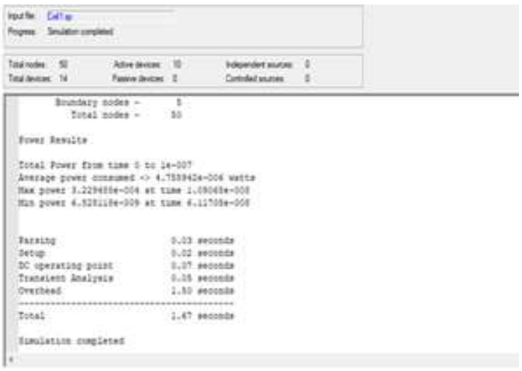


Fig.2 Modified Hybrid Full Adder On S-Edit



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Input file:  Cell1.sp
Progress:    Simulation completed

Total nodes:    50     Active devices:   10     Independent sources:   0
Total devices:  14     Passive devices:  0      Controlled sources:    0

      Boundary nodes =       5
         Total nodes =      50

Power Results

Total Power from time 0 to 1e-007
Average power consumed -> 4.755942e-006 watts
Max power 3.229485e-004 at time 1.09048e-008
Min power 4.528118e-009 at time 6.11708e-008


Parsing                         0.03 seconds
Setup                           0.02 seconds
DC operating point              0.07 seconds
Transient Analysis              0.05 seconds
Overhead                        1.30 seconds
-----------------------------------------
Total                           1.47 seconds

Simulation completed
```

Fig.3 Modified Hybrid Full Adder On T-Spice

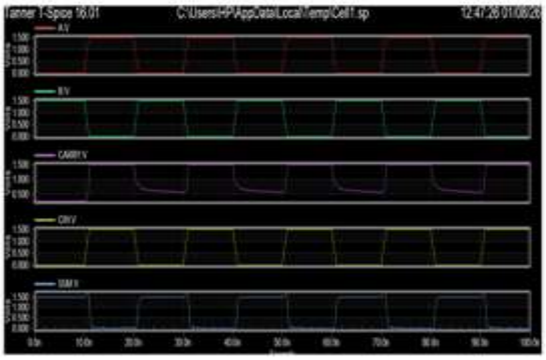

Fig.4 Modified Hybrid Full Adder On W—Edit

VI CONCLUSION

This research presents a one-bit hybrid modified full adder that successfully addresses the critical challenges of low power consumption and high-speed operation, which are essential in modern VLSI systems and portable electronics. By integrating a hybrid logic approach combining GDI, pass-transistor logic, and static CMOS, the design achieves an optimal balance between transistor count, switching activity, and output stability, ensuring full-swing outputs and robust operation under low-voltage conditions. The carry and sum generation paths have been carefully optimized to minimize critical path delay, resulting in faster propagation and enabling reliable cascaded operation in multi-bit adders such as ripple-carry and carry-lookahead structures. Power efficiency is further enhanced by reducing short-circuit and leakage currents, making the design suitable for ultralow-voltage applications. Simulation and analysis demonstrate significant improvements in power-delay product (PDP) and energy-delay product (EDP) compared to conventional CMOS and previously proposed full adder architectures, confirming that the design is both energy-efficient and high-performing. In addition, the reduced transistor count and simplified interconnections contribute to a compact layout, smaller silicon area, and lower parasitic capacitances, which are critical for integration into complex arithmetic units, digital signal processing cores, and system-on-chip designs. The proposed hybrid modified full adder is also fully compatible with standard CMOS fabrication processes, enabling easy adoption in existing VLSI design flows without requiring specialized manufacturing techniques. Overall, this work provides a scalable, reliable, and high-performance full adder solution that meets the demands of modern low-power, high-speed applications, making it ideal for energy-constrained systems such as IoT devices, wearable electronics, and portable computing platforms.

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