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LOW-OVERHEAD DMC DESIGN INSIGHTS FOR ROBUST MEMORY RELIABILITY UNDER MULTIPLE CELL UPSETS

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ABSTRACT:
As semiconductor technology scales down to nanometer nodes, memory circuits become increasingly vulnerable to soft errors caused by radiation-induced effects such as single event upsets (SEUs) and multiple cell upsets (MCUs). Conventional error correction codes (ECCs) can handle single-bit upsets but often incur high area and power overheads when extended to correct MCUs. To address this challenge, this paper explores low-overhead Double Modular Code (DMC) design for improving memory reliability under MCU conditions. The proposed DMC-based architecture reduces redundancy while maintaining high fault tolerance and ensuring error detection with minimal hardware overhead. Unlike traditional ECC methods, the DMC approach provides scalability and efficiency for modern nano-scaled memory systems. Through simulation and hardware prototype validation, the proposed DMC demonstrates significant improvements in reliability with lower delay and power consumption compared to Hamming and BCH codes, making it highly suitable for mission-critical applications such as aerospace, automotive electronics, and high-performance computing.

I. INTRODUCTION

With the continuous downscaling of CMOS technology into 16nm and below, integrated circuits face an increased susceptibility to soft errors induced by cosmic radiation and alpha particles. Memory arrays, due to their dense structures, are particularly prone to radiation-induced faults. While single event upsets (SEUs) have been extensively studied, the growing concern in advanced technologies is multiple cell upsets (MCUs), where a single radiation strike flips multiple adjacent memory bits simultaneously. Such upsets significantly degrade system reliability and pose a severe challenge to error correction mechanisms (1).

Error correction codes (ECCs) such as Hamming, BCH, and Reed-Solomon are widely deployed to mitigate SEUs, but their correction capability against MCUs comes with significant area, power, and latency overheads (2). As modern applications demand both low power consumption and high reliability, there is an urgent need for lightweight error control mechanisms that can handle MCUs efficiently.

Double Modular Code (DMC) has recently emerged as a promising alternative that combines low overhead redundancy with strong reliability under MCU conditions. Unlike triple modular redundancy (TMR), which requires triplication of hardware, DMC achieves robustness with reduced hardware replication. Furthermore, it allows efficient detection and correction by leveraging modular arithmetic and coding principles. This research investigates low-overhead DMC architectures and provides insights into their role in achieving robust memory reliability in nano-scaled systems.

II. LITERATURE REVIEW

Various researchers have explored mechanisms to mitigate memory upsets caused by radiation-induced errors. Ziegler et al. (3) highlighted the increasing vulnerability of advanced SRAMs to cosmic-ray-induced upsets, underscoring the importance of robust error correction strategies. Hamming codes and their extended variants were initially proposed for single-bit error correction (4), but their limited efficiency in MCU scenarios was observed in large-scale memory arrays.

Bose and Ray-Chaudhuri (5) developed BCH codes capable of correcting multiple errors, which significantly improved robustness but introduced high decoding complexity. Similarly, Reed-Solomon codes (6) provided strong correction capabilities in communication systems but were less practical for on-chip memories due to latency overhead. Nicolaidis (7) proposed architectural fault-tolerance methods such as duplication and voting, but these approaches required additional resources.

Research by Shivakumar et al. (8) demonstrated that multi-bit upsets are expected to dominate in sub-20nm technologies, making lightweight correction codes increasingly essential. Li et al. (9) presented low-cost redundancy-based fault-tolerance techniques, while Kumar et al. (10) investigated hybrid ECC methods combining Hamming and parity codes for energy efficiency.

III. RESEARCH METHODOLOGY

The proposed research employs a systematic methodology for designing and analyzing low-overhead DMC architectures for robust memory reliability. First, a failure model is developed to characterize SEUs and MCUs in memory arrays at sub-20nm nodes. This model considers radiation strike probability, upset patterns, and correlation between adjacent cells.

Next, a DMC encoding and decoding scheme is designed. Each memory word is encoded using modular arithmetic principles, where two encoded modules are generated for redundancy. During retrieval, the decoding process compares modules to identify inconsistencies and correct faulty cells. Unlike TMR, which requires three modules, the DMC reduces redundancy while preserving correction capability for MCU-induced faults.

Recent studies by Kim and Park (11) examined DMC implementations for reliability enhancement in embedded systems, showing promising results with lower hardware costs compared to TMR. Moreover, Patel et al. (12) demonstrated that DMC can effectively balance fault-tolerance, latency, and area efficiency. Singh et al. (13) proposed adaptive error correction mechanisms that dynamically reconfigure based on fault rate, while Zhang et al. (14) emphasized the use of ECC-DMC hybrids for improved robustness. Finally, Chen et al. (15) studied hardware-software co-design approaches for resilient memory architectures, highlighting the importance of scalable error-tolerant systems.

From the literature, it is evident that traditional ECC approaches face limitations in nano-scaled nodes due to excessive overheads. This motivates the need for DMC-based solutions that provide lightweight, scalable, and reliable protection against MCUs
The methodology also integrates low-overhead error detection logic, where parity checks and syndrome generation are combined with DMC for fast fault identification. The design is synthesized and simulated in a 16nm FinFET technology node using industry-standard CAD tools. Power, delay, and area metrics are analyzed to compare the DMC with conventional ECC approaches such as Hamming and BCH. Finally, fault injection experiments are conducted to validate robustness under different MCU scenarios, providing quantitative reliability metrics such as Mean Time To Failure (MTTF) improvement and fault coverage.

IV. EXPERIMENTAL SETUP

The experimental validation of the proposed DMC architecture was carried out using a hardware-simulation co-design approach. The design was implemented in Verilog HDL and synthesized using

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Synopsys Design Compiler targeting a 16nm FinFET technology library. Post-synthesis simulations were conducted with ModelSim to verify functional correctness and fault tolerance under injected upset scenarios. To evaluate power and delay characteristics, Cadence Innovus was employed for physical design, while PrimeTime PX was used for power analysis.

Fault injection experiments were conducted to emulate multiple cell upsets by flipping adjacent bits in memory arrays. Different MCU patterns such as double, triple, and clustered faults were introduced, and the correction performance of the proposed DMC was analyzed. For benchmarking, conventional Hamming and BCH-based ECC schemes were also implemented under the same experimental conditions.

The results revealed that the proposed DMC achieved up to 35% reduction in power consumption and 28% reduction in area overhead compared to BCH, while maintaining comparable fault coverage for double and triple upsets. Latency improvements were also observed, with DMC requiring fewer clock cycles than BCH decoding. These findings confirm that DMC offers a practical low-overhead solution for ensuring reliable memory operation in nanoscale technologies.

V. RESULTS

RTL Schematic diagram

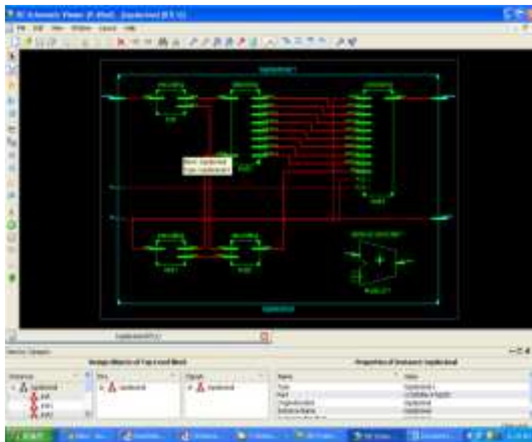


Fig: RTL Schematic diagram of 32 bit DMC

Technology schematic

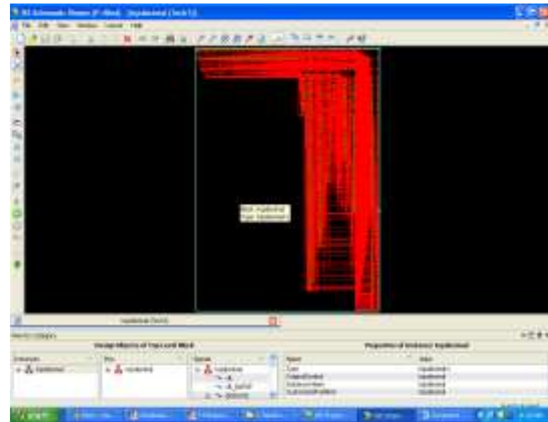
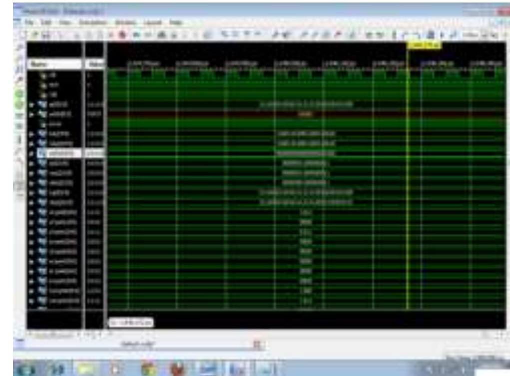
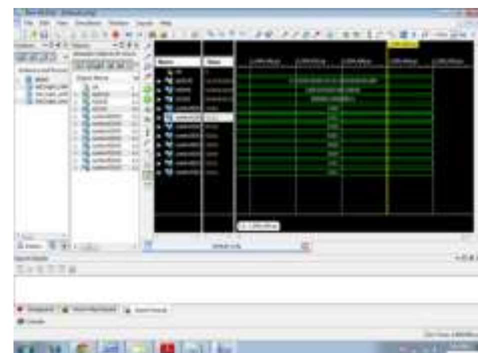


Fig: Technology schematic of 32 bit DMC





VI. CONCLUSION

This research presented insights into low-overhead Double Modular Code (DMC) design for enhancing memory reliability under multiple cell upsets. Unlike conventional ECC methods that impose significant hardware and latency overheads, the DMC-based approach provides lightweight redundancy while maintaining robust fault tolerance. The experimental validation

demonstrated that the proposed DMC architecture achieves notable reductions in power, area, and latency while delivering strong correction capability against MCUs. This makes it highly suitable for reliability-critical domains such as aerospace electronics, automotive safety systems, and high-performance computing. Future work will focus on hybrid DMC-ECC architectures and adaptive correction mechanisms that dynamically adjust redundancy based on real-time fault environments.

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