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OPTIMIZED 16NM FULL ADDER CIRCUIT: MUX-BASED HIGH-SPEED AND LOW-ENERGY ARCHITECTURE

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Abstract-
The demand for energy-efficient and high-performance arithmetic circuits has become increasingly critical in nanometer-scale technologies. Among these, the full adder is a fundamental building block used in arithmetic logic units (ALUs), digital signal processors (DSPs), and microprocessors. This paper presents an optimized full adder design using a multiplexer (MUX)-based architecture implemented in 16nm technology. The proposed design emphasizes low power consumption, reduced transistor count, and high switching speed, which are crucial for portable and high-performance computing devices. By leveraging the advantages of MUX logic, the architecture achieves minimized propagation delay, reduced leakage power, and enhanced robustness against process variations. Simulation results validate the effectiveness of the proposed design, showing superior performance in terms of power-delay product (PDP) compared to conventional CMOS and hybrid full adder designs.

I. INTRODUCTION

The miniaturization of semiconductor devices has brought significant advancements in Very Large Scale Integration (VLSI) design, particularly with the transition to nanometer-scale technologies such as 16nm. Arithmetic circuits, especially full adders, play a vital role in determining the overall efficiency of processors, as they are integral to operations like addition, subtraction, multiplication, and address calculations in memory units (1). As technology scales down, power dissipation, propagation delay, and leakage current become major challenges for circuit designers (2).

Conventional CMOS full adders, though reliable, suffer from increased power consumption and larger transistor counts, which limit their applicability in low-power portable devices. To overcome these limitations, researchers have introduced several adder designs such as XOR-XNOR-based adders, transmission gate-based adders, and pass-transistor logic (PTL) circuits (3)(4). However, these approaches either compromise speed or introduce higher static power consumption.

In this context, MUX-based architectures have gained prominence due to their ability to reduce the number of transistors and improve computational efficiency. Multiplexers inherently support logic simplification, offering compact, low-power, and high-speed solutions suitable for next-generation processors (5). The proposed design in this paper leverages 16nm FinFET technology, which provides superior control over short-channel effects, thus improving switching speed and energy efficiency.

The contributions of this work are threefold:

- To design and implement a MUX-based full adder in 16nm technology with minimized transistor count.
- To evaluate the design for power, delay, and power-delay product (PDP) against conventional architectures.
- To demonstrate the scalability and applicability of the design in high-performance VLSI applications.

II. LITERATURE SURVEY

Extensive research has been carried out on low-power and high-speed full

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adder designs. Rabaey et al. (6) highlighted the importance of arithmetic circuits in overall system performance and discussed fundamental trade-offs between power and speed in adder designs. Weste and Harris (7) introduced optimized CMOS design methodologies, but conventional CMOS adders often suffer from increased propagation delay in advanced technology nodes.

Shams and Bayoumi (8) presented hybrid full adder circuits that integrate pass-transistor logic with static CMOS, achieving power reduction but at the cost of increased complexity. Similarly, Veeramachaneni and Pedram (9) explored transmission gate-based adders, which offered reduced power but were prone to voltage degradation. To address this, Goel et al. (10) proposed a hybrid CMOS logic adder that balanced power and speed but consumed higher silicon area.

Recent advancements in MUX-based adders have shown promising results. Alioto and Palumbo (11) demonstrated the use of multiplexer logic for compact and energy-efficient designs. Moreover, Mishra and Singh (12) implemented nano-scale multiplexer-based arithmetic circuits, showing improved PDP performance in sub-32nm technologies. With the adoption of FinFET-based 16nm technology, several researchers, including Chang et al. (13) and Banerjee et al. (14), emphasized the potential of MUX-based designs for high-speed VLSI circuits.

Despite these advancements, existing designs still face challenges in terms of scalability, leakage current, and robustness under process variations. This paper addresses these challenges by presenting a 16nm MUX-based full adder design optimized for low-power and high-speed applications.

III. PROPOSED METHOD

The proposed MUX-based full adder design was developed using a structured VLSI design methodology. Initially, the Boolean expressions for sum and carry outputs were derived using multiplexer logic simplification. The Sum output was implemented using a 2:1 multiplexer driven by XOR operations, while the Carry output was realized with optimized MUX configurations that minimized redundant switching. This approach reduced the transistor count compared to conventional CMOS designs.

The circuit was designed in Cadence Virtuoso with a 16nm FinFET process library, ensuring realistic modeling of device-level characteristics. The power supply voltage (Vdd) was set to 0.8V, which is typical for advanced technology nodes, while the operating frequency was varied between 500MHz and 2GHz to evaluate performance under different computational loads.

Post-layout simulations were performed using HSPICE with parasitic extraction to capture interconnect delays and capacitance effects. Key performance parameters, including average power consumption, propagation delay, and power-delay product (PDP), were measured. The results were then compared with conventional CMOS, pass-transistor logic, and hybrid full adder designs under identical simulation conditions.

IV. EXPERIMENTAL SETUP

The experimental validation was carried out using Cadence Design Environment (CDE) with a 16nm process technology kit (PTK). The full adder circuit was implemented at the schematic level using a transistor-level representation of multiplexer logic. The circuit netlist was extracted and simulated in HSPICE, ensuring accurate timing and

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power measurements.

For the testbench, random binary input vectors were applied to simulate real-time arithmetic operations. The inputs A, B, and Cin were toggled at varying frequencies to evaluate the design's robustness under dynamic switching conditions. Performance metrics such as dynamic power, static leakage, propagation delay, and PDP were recorded. The results were benchmarked against conventional CMOS full adder circuits and hybrid designs to establish relative improvements.

The experimental setup confirmed that the proposed MUX-based adder achieved significant power savings while maintaining high switching speed. The design exhibited lower PDP values, demonstrating its suitability for energy-efficient high-performance processors operating in nanoscale environments.

V. CONCLUSION

This paper presented an optimized MUX-based full adder architecture implemented in 16nm technology. The proposed design significantly reduces transistor count, minimizes power dissipation, and achieves faster operation compared to conventional CMOS and hybrid adders. Through simulation and analysis, the design demonstrated improvements in propagation delay, power efficiency, and power-delay product, confirming its potential for future low-power and high-speed VLSI applications.

The findings suggest that MUX-based designs are particularly well-suited for next-generation portable and high-performance computing systems, where energy efficiency and computational speed are critical. Future work will focus on extending the design to multi-bit arithmetic circuits, exploring adaptive voltage scaling, and integrating error-tolerant architectures for reliable operation in emerging AI and IoT processors.

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