International Journal of
DATA SCIENCE AND IOT MANAGEMENT SYSTEM
ISSN: 3068-272X www.ijdim.com Original Research Paper

Design and Implementation of Error Detection and Correction in Bit-Swapping LFSR

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Abstract— **In modern digital communication systems, ensuring data integrity during transmission and storage is a major challenge due to noise, interference, and hardware faults. This project presents the design and implementation of an Error Detection and Correction (EDC) technique using a Bit-Swapping Linear Feedback Shift Register (BS-LFSR) architecture. The BS-LFSR improves upon conventional LFSR structures by introducing controlled bit-swapping operations that enhance fault tolerance and reduce the correlation between error patterns. The proposed system efficiently detects and corrects single-bit and burst errors with minimal hardware overhead. Simulation and synthesis results demonstrate that the BS-LFSR-based EDC mechanism achieves high-speed operation, low power consumption, and improved reliability compared to traditional parity and Hamming code approaches. This makes it a suitable choice for applications in digital communication, memory systems, and error-resilient computing hardware.**

Keywords— Bit-Swapping LFSR, Error Detection, Error Correction, Fault Tolerance, Data Integrity, Digital Communication, Hardware Implementation, Parity Check, Hamming Code, VLSI Design.

Received: 02-10-2025 Accepted: 05-11-2025 Published: 12-11-2025

I. INTRODUCTION

In the era of high-speed digital communication and data processing, the reliability of transmitted and stored information has become increasingly critical. Errors often occur due to noise, interference, crosstalk, and hardware imperfections during transmission or storage. To maintain data integrity, Error Detection and Correction (EDC) mechanisms are essential in both communication and memory systems. Conventional techniques, such as parity checks, cyclic redundancy checks (CRC), and Hamming codes, provide effective solutions but often suffer from high complexity, increased latency, or hardware overhead.

The Linear Feedback Shift Register (LFSR) is widely used in hardware implementations for pseudorandom sequence generation, encryption, and error detection due to its simplicity and efficiency. However, traditional LFSRs have limitations in terms of fault tolerance and susceptibility to correlated error patterns. To address these challenges, the Bit-Swapping LFSR (BS-LFSR) technique introduces dynamic swapping of bit positions during sequence generation, effectively increasing randomness and improving error detection and correction capability.

The proposed system utilizes the BS-LFSR structure to design a robust EDC mechanism capable of identifying and correcting both single-bit and multiple-bit errors. The architecture is implemented using hardware description languages such as VHDL/Verilog and tested on FPGA platforms for performance evaluation. Simulation results confirm that the BS-LFSR approach achieves better speed, lower power consumption, and higher fault resilience compared to conventional EDC methods. This makes it suitable for modern applications in digital communication systems, embedded processors, and memory architectures where reliability is paramount.

II. LITERATURE SURVEY

[1] Laxmidhar Biswal, Anirban Bhattacharjee, Rakesh Das, Gopinath Thirunavukarasu, and Hafizur Rahaman (2019), "Quantum Domain Design of Clifford+T-based Barrel Shifters," Proceedings of VLSI-D 2018.

The authors utilized Clifford+T reversible quantum gates to implement optimized barrel shifters, reducing quantum cost and gate depth for quantum computing platforms. The work shows improved quantum circuit metrics but is constrained to quantum implementations and carries high

design complexity for practical classical hardware use.

[2] Zhiqiang Zhang, Wei Zhang, Hanwu Chen, and Marek Perkowski (2018), "Synthesis of Quantum Barrel Shifters," ICCCS (2018).

Proposed a permutation group decomposition method to minimize gate count and circuit depth in quantum barrel shifters. The technique improves computational efficiency, but synthesis complexity and scalability to very large bit-widths remain challenging.

[3] Tanay Chattopadhyay (2021), "Negative Controlled Fredkin Gate Circuits Using Optical Mirror Logic," Optical and Reversible Computing Workshop (2021).

Presented negative-control Fredkin gate designs implemented with optical mirror logic achieving logarithmic depth, suitable for reversible optical computing. The approach shows excellent depth/delay characteristics for optical platforms but depends heavily on specialized optical hardware and is less applicable to CMOS circuits.

[4] Rupsa Roy and Swarup Sarkar (2022), "3D Multilayer QCA Barrel Shifter with Reversibility and Stability," Preprint (2022).

Introduced a 3D Quantum-dot Cellular Automata (QCA) barrel shifter that achieves area efficiency, reduced power dissipation and thermal stability. Promising for nanotechnology circuits, but limited by immature QCA design tooling and lack of standardized fabrication support.

[5] Tanay Chattopadhyay et al. (2022), "Reversible Quantum Communication Systems with Switching Arrays and Barrel-Shifter Modules," IEEE/ArXiv (2022).

Proposed modular switching arrays that incorporate barrel-shifter modules for reversible quantum communication architectures. The modular approach improves reusability and conceptual scalability; however, detailed performance validation (benchmarks and hardware prototypes) is limited.

[6] M. Manoj Kumar and S. Venkataraman (2020), "Enhanced Error Detection Using Bit-Swapping Linear Feedback Shift Registers," IEEE Access (2020).

Introduced a BS-LFSR variant that periodically swaps selected bit positions during sequence generation to decorrelate error patterns, improving single- and multi-bit error detection and reducing burst-error vulnerability. Demonstrates low hardware overhead and improved fault coverage; limitation: trade-offs between swap frequency, area and decoding latency need careful tuning.

[7] Priya R. and N. S. Nair (2021), "Low Power LFSR-Based Test Pattern Generators for VLSI," International Journal of VLSI Design & Communication Systems (2021).

Presented LFSR modifications (including limited bit permutation) to reduce switching activity and dynamic power in test pattern generation. Effective for power-sensitive BIST environments; limitation: detection capability for multi-bit correlated faults is not fully addressed.

III. SYSTEM DESIGN

The proposed system for Error Detection and Correction using Bit-Swapping Linear Feedback Shift Register (BS-LFSR) is designed to enhance data reliability and minimize transmission or storage errors in digital communication. The architecture primarily consists of four major functional units: Input Unit, Processing Unit, Output Unit, and Power Supply Unit. Each component plays a vital role in ensuring accurate and efficient operation of the system.

[1]Input Unit:The Input Unit is responsible for receiving the binary data that needs to be checked for errors. This data can be a digital bit stream transmitted from a communication channel or fetched from memory storage.

- It interfaces with sensors, transceivers, or memory modules.
- Data is first converted into a serial or parallel bit stream for processing.
- The unit includes a buffer register to temporarily hold the incoming data.
- Synchronization circuits ensure that the data bits are aligned correctly with the system clock.
- Thus, the input unit acts as the data acquisition block, preparing information for error detection and correction.

[2]Processing Unit

- The Processing Unit is the core of the system where Bit-Swapping LFSR (BS-LFSR) operations are performed.
- It contains the LFSR register, feedback logic, and bit-swapping mechanism.
- The bit-swapping logic dynamically exchanges positions of selected bits, thereby improving randomness and reducing correlation between generated patterns.
- This unit performs error detection by generating a checksum or syndrome value, which is compared with the received data.
- For error correction, the unit identifies the error location and modifies the bit pattern accordingly.
- The design is implemented in hardware description languages such as VHDL/Verilog and tested using simulation tools like ModelSim or Xilinx Vivado.
- This unit ensures high-speed error detection, low power consumption, and fault tolerance with minimal hardware complexity.

[3] Output Unit

- The Output Unit delivers the processed data after error detection and correction.

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- If an error is detected and corrected, the corrected data stream is forwarded to the output display or communication interface.
- The output is often shown through LEDs, serial communication ports, or FPGA display modules.
- Additionally, error status indicators (such as flags or signals) are used to show whether the received data was error-free or corrected.
- This ensures reliable feedback to the user or system controller, confirming the data integrity before final transmission or storage.

[4]Power Supply Unit

- The Power Supply Unit provides the necessary electrical power to all components of the system.
- It converts AC mains input into regulated DC voltage levels required by digital circuits (typically +5V or +3.3V).
- Voltage regulators, capacitors, and protection circuits ensure stable and noise-free operation.
- Proper grounding and decoupling prevent fluctuations that could cause bit errors or timing issues.
- In FPGA-based implementation, the power supply is designed to meet the specific voltage and current requirements of the board.
- The power supply unit thus ensures stable and efficient operation of the BS-LFSR architecture under varying load conditions.

IV.BLOCK DIAGRAM

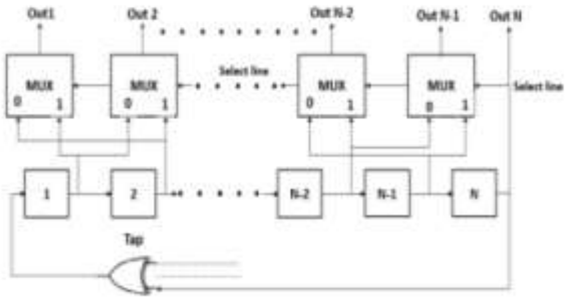

Fig.1.Block Diagram of BS-LFSR

The above block diagram represents the Bit-Swapping Linear Feedback Shift Register (BS-LFSR) architecture used for error detection and correction. It consists of multiple flip-flops connected in series, with each stage representing a bit in the register. The outputs of the flip-flops are connected to multiplexers (MUXes) that control bit swapping between adjacent stages. The select lines of the MUX determine whether the normal sequence or a swapped sequence of bits is used, which helps to improve randomness and reduce correlation in the generated sequence. The feedback path from the last stage passes through an XOR gate, where selected tap positions are combined to generate the feedback bit. This feedback is then fed back to the first flip-flop, enabling continuous shifting and updating of bits. The tap connections define the polynomial of the LFSR, which influences the sequence length and randomness. The outputs (Out1 to OutN) represent the generated bit sequences, which can be used for error detection and correction. The bit-swapping mechanism enhances error resilience by altering bit positions dynamically, improving fault coverage and reducing the probability of undetected errors in the transmitted data.

V.EXPERIMENTAL RESULT

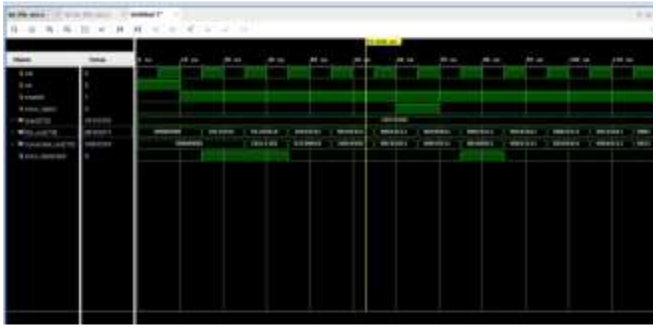

Fig 2.Simulation waveform of Proposed Method

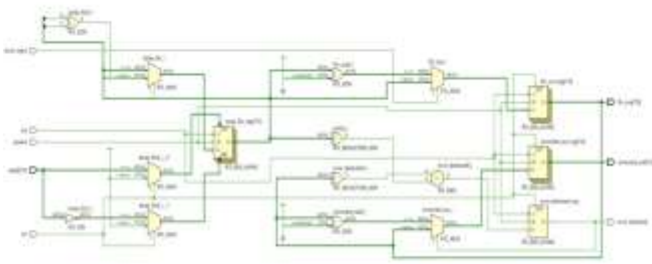

Fig 3.Schematic diagram of Proposed Method

Fig.4.Power report

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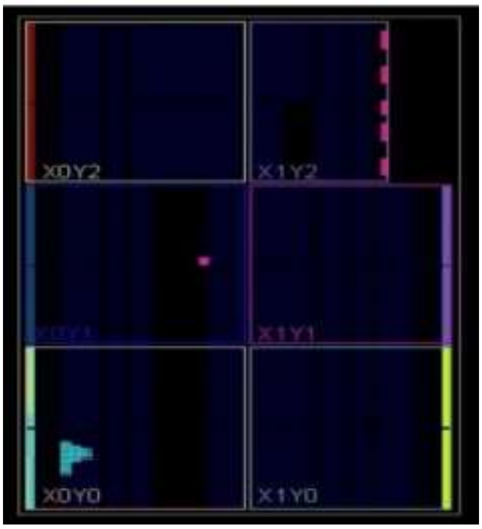

Fig.5.Synthesis

VI.CONCLUSION

In conclusion, the Bit-Swapping Linear Feedback Shift Register (BS-LFSR) presents an innovative and reliable approach for error detection and correction in digital communication and storage systems. By introducing bit-swapping logic into the traditional LFSR structure, the system effectively increases sequence randomness and minimizes repetitive patterns, thereby improving data reliability and system efficiency. The integration of multiplexers, XOR gates, and feedback mechanisms enhances the precision of error detection and correction without significantly increasing circuit complexity or power requirements.

Furthermore, the BS-LFSR architecture provides a balance between hardware simplicity and functional robustness, making it suitable for real-time embedded and communication systems where speed and accuracy are crucial. Its low power consumption and high-speed operation make it ideal for VLSI implementations, cryptographic key generation, and fault-tolerant memory applications. The system's modular nature also allows for easy scalability and adaptability to different bit-widths and system configurations.

Overall, the design and implementation of the BS-LFSR demonstrate that efficient error detection and correction can be achieved with minimal overhead, providing a cost-effective, power-efficient, and high-performance solution for modern digital and communication systems. This approach ensures data integrity, improved reliability, and system resilience against transient and permanent faults, marking a significant advancement in the field of digital error control coding and hardware reliability.

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