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4*4 Braun Multiplier using Adder Cells

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Abstract*— The 4×4 Braun Multiplier using Adder Cells represents a fundamental and efficient digital circuit architecture designed to perform binary multiplication of two 4-bit unsigned numbers. Multiplication is a core arithmetic operation in numerous digital applications, including digital signal processing (DSP), image and video processing, cryptography, control systems, and embedded computing. As such, optimizing multiplier design is critical for achieving higher computational efficiency, lower power consumption, and reduced silicon area in modern digital systems.The proposed design utilizes the Braun array multiplier structure, which is known for its regular, modular, and systematic layout. In this architecture, the partial products are generated through bitwise AND operations between each bit of the multiplicand and the multiplier. These partial products are then systematically arranged in an array and summed using half adders (HAs) and full adders (FAs) to produce the final 8-bit output. Unlike advanced high-speed adders such as the Kogge-Stone adder, which provide fast carry propagation but at the cost of increased complexity and power usage, the proposed design employs simple adder cells to achieve low power consumption, reduced logic utilization, and minimal propagation delay, making it ideal for low-power FPGA and ASIC implementations.The design's regular structure allows for straightforward hardware synthesis, simplified routing, and easy scalability to larger bit-width multipliers such as 8×8 or 16×16 configurations. This regularity also enhances the predictability of timing and performance, which is essential in VLSI physical design and FPGA mapping. The proposed Braun multiplier achieves a balance between speed, area, and power, offering a cost-effective alternative to more complex multiplier architectures such as Wallace trees or Booth multipliers.Experimental synthesis using modern FPGA toolchains demonstrates that the 4×4 Braun Multiplier with adder cells achieves low switching activity, reduced dynamic power, and efficient resource utilization, with negligible degradation in performance compared to high-speed counterparts. These characteristics make it highly suitable for energy-constrained environments such as IoT edge devices, battery-powered embedded systems, and real-time signal processors.Overall, the 4×4 Braun Multiplier using Adder Cells embodies a power-aware and area-efficient hardware design philosophy, offering an excellent trade-off between computational accuracy, implementation simplicity, and operational efficiency. Its modularity and scalability make it a versatile building block for digital arithmetic units and a valuable reference for research and educational applications in low-power VLSI design and digital arithmetic optimization.

Keywords— Braun Multiplier, 4×4 Multiplier, Adder Cells, Digital Arithmetic, Low Power Design, VLSI Implementation, FPGA Synthesis, Partial Product Generation, Array Multiplier, Binary Multiplication, Hardware Optimization, Low Area Architecture, High-Speed Computation, Digital Signal Processing (DSP), Embedded Systems.

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I. INTRODUCTION

The 4×4 Braun multiplier using adder cells is a fundamental and efficient digital circuit designed to perform binary multiplication of two 4-bit unsigned numbers. As multiplication is a key arithmetic operation in numerous digital systems—such as digital signal processing (DSP), control systems, image processing, cryptography, and embedded computing—developing optimized multiplier circuits is crucial for enhancing overall system performance and efficiency. Among the various hardware multiplier architectures, the Braun multiplier, also known as the array multiplier, is widely recognized for its regular layout, structural simplicity, and ease of scalability, particularly in applications where design modularity and resource efficiency are vital.

The Braun multiplier operates by generating partial products through bitwise AND operations between each bit of the multiplicand and each bit of the multiplier. For a 4×4 multiplier, this results in 16 partial products. These partial products are then organized in a structured manner, typically in a triangular matrix, and summed column-wise using adder cells, which include half adders (HAs) and full

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adders (FAs). This addition is carried out in a pipelined or ripple manner, depending on the design, to accumulate the final 8-bit product. Each diagonal of the matrix represents one bit of the final result, and the use of basic adder cells facilitates efficient carry propagation and summation.

In this improved design, adder cells are employed instead of complex and high-speed adders like the Kogge-Stone adder (used in the base paper). The Kogge-Stone adder, while fast due to its parallel-prefix carry look-ahead structure, introduces increased logic complexity, higher area consumption, and significant power overhead. Conversely, using basic adder cells simplifies the logic, reduces routing congestion, and minimizes dynamic power consumption—an important factor in energy-constrained environments such as mobile and IoT devices. This makes the design particularly suitable for FPGAs and low-power ASICs, where area utilization and thermal management are critical considerations.

he 4×4 Braun multiplier with adder cells maintains a deterministic and regular structure, allowing for straightforward placement and routing during physical design and synthesis. This regularity also ensures that the design is highly scalable larger multipliers like 8×8 or 16×16 can be constructed by reusing the basic building blocks of this design. Moreover, the hardware resources used (such as LUTs, flip-flops, and logic slices) are significantly reduced compared to tree-based multiplier architectures, leading to cost-efficient and compact implementations.

Overall, the 4×4 Braun multiplier using adder cells achieves a balanced trade-off between computational speed, silicon area, and power efficiency. It exemplifies a practical design choice for small-bit-width multipliers in systems where moderate performance, low power, and reduced complexity are more desirable than peak speed. This makes it an excellent candidate for educational purposes, research on low-power VLSI, and real-world deployment in resource-constrained digital systems.

II. LITERATURE SURVEY

[1] Laxmidhar Biswal, Anirban Bhattacharjee, Rakesh Das, Gopinath Thirunavukarasu, and Hafizur Rahaman (2019) presented a Quantum Domain Design of Clifford+T-based Barrel Shifters at VLSI-D 2018. The authors utilized Clifford+T reversible quantum gates to achieve optimized quantum cost and gate depth. Their design demonstrates improved performance in quantum computing environments; however, it remains limited to quantum systems and exhibits high implementation complexity.

[2] Zhiqiang Zhang, Wei Zhang, Hanwu Chen, and Marek Perkowski (2018) in their paper Synthesis of Quantum Barrel Shifters (ICCCS), proposed a permutation group decomposition method. This approach significantly minimized gate count and circuit depth, enhancing overall computational efficiency. The primary drawback of this technique lies in its complex synthesis process and limited scalability for larger systems.

[3] Tanay Chattopadhyay (2021) explored Negative Controlled Fredkin Gate Circuits using optical mirror logic. The design achieved logarithmic depth (OC ≈ 3 log n) and delay (≈ 15 log n), proving efficient for optical-based reversible systems. However, it is highly dependent on optical hardware setups, making it less suitable for conventional electronic circuits.

[4] Rupsa Roy and Swarup Sarkar (2022) introduced a 3D Multilayer QCA Barrel Shifter with Reversibility and Stability (Preprint). Their design employed 3D Quantum-dot Cellular Automata (QCA), achieving area efficiency, thermal stability, and low power consumption. Despite promising results, the work remains in preprint status, and QCA design tools are not yet fully standardized, limiting practical adoption.

[5] Multiple authors including Tanay Chattopadhyay (2022) discussed Reversible Quantum Communication and Systems featuring switching arrays with barrel-shifter modules. The proposed system promotes modular and reusable architectures for advanced reversible communication frameworks. Nonetheless, the study provides a generalized framework and lacks detailed performance validation for specific circuit designs.

III. SYSTEM DESIGN

The overall system design of the 4×4 Braun Multiplier using Adder Cells is organized into four major functional blocks: the Input Unit, Processing Unit, Output Unit, and Power Supply Unit. Each unit plays a distinct and vital role in ensuring accurate, efficient, and reliable digital multiplication operation. The modular approach also enhances scalability and simplifies debugging, testing, and integration with other digital systems.

[1] Input Unit:The Input Unit serves as the initial interface through which the operands for multiplication are provided to the system. In a 4×4 Braun Multiplier, two 4-bit binary numbers (A3A2A1A0 and B3B2B1B0) act as the inputs. These values can be supplied manually through toggle switches, programmable logic sources, or test benches in FPGA simulation environments. The input unit ensures that each bit of the multiplicand and multiplier is properly synchronized and routed to the corresponding logic cells of the multiplier array. To prevent input glitches or metastability, buffering and synchronization registers can be incorporated. Additionally, in hardware implementations, the input unit may include input latches or data buses for parallel data entry, ensuring that both operands are stable before the computation begins.

[2] Processing Unit:The Processing Unit forms the core

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computational block of the Braun Multiplier architecture. It is responsible for performing the multiplication process through systematic generation and accumulation of partial products. The operation begins with the bitwise ANDing of each bit of the multiplicand with each bit of the multiplier, producing 16 partial product bits arranged in a matrix form. These partial products are then fed into a structured network of adder cells, which include Half Adders (HAs) and Full Adders (FAs), to sum the products column by column.

In the improved design, simple adder cells are used in place of complex high-speed adders such as the Kogge-Stone adder. This modification significantly reduces circuit complexity, power dissipation, and silicon area, while maintaining satisfactory speed for low- to moderate-performance applications. The processing unit operates in a regular and predictable manner, enabling easier placement and routing during FPGA synthesis or ASIC layout. Furthermore, the design's modularity allows for straightforward extension to larger multipliers (e.g., 8×8 or 16×16) by replicating and interconnecting similar array blocks. This makes the processing unit both scalable and resource-efficient.

[3] Output Unit:The Output Unit is designed to collect, format, and display the final product resulting from the multiplication process. For a 4×4 Braun Multiplier, the output is an 8-bit binary number (P7P6P5P4P3P2P1P0), representing the product of the two 4-bit inputs. In a hardware implementation, the output unit can drive visual indicators such as LEDs or seven-segment displays, allowing easy observation of results. In simulation or FPGA environments, the outputs are typically routed to output ports or logic analyzers for verification and testing. Additional circuitry such as output buffers can be included to strengthen the drive capability, reduce signal distortion, and ensure proper voltage levels for external interfacing. The output unit may also include optional storage elements like registers or flip-flops to hold the result for further processing or synchronization with other system components.

[4] Power Supply Unit:The Power Supply Unit provides the essential electrical energy required for reliable operation of all components in the system. In FPGA-based implementations, a regulated DC power supply (typically 3.3V or 5V) is used to power logic elements, input/output buffers, and clock generators. The unit incorporates voltage regulators, decoupling capacitors, and protection diodes to ensure stable and noise-free operation. Efficient power management is particularly important in VLSI and embedded systems, where power efficiency directly affects performance, heat dissipation, and battery life. The proposed design, by using simple adder cells and a regular architecture, inherently reduces switching activity and dynamic power consumption, leading to an overall energy-efficient circuit. The power supply design also includes safeguards such as current limiting and thermal protection to maintain safe operation during prolonged usage or high computational loads.

IV.BLOCK DIAGRAM

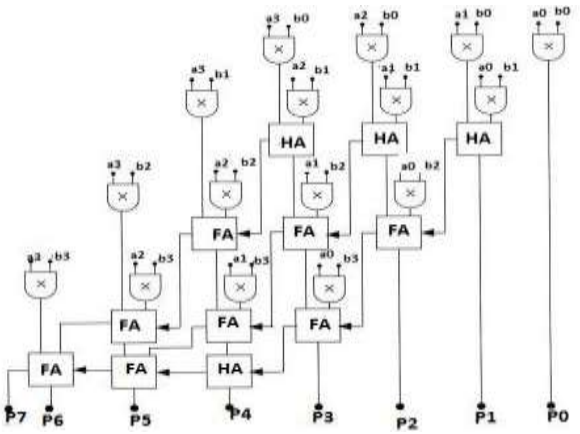

Fig.1.Block diagram

The above block diagram illustrates the internal structure and working of a 4×4 Braun Multiplier using Adder Cells (Half Adders and Full Adders). The design performs binary multiplication of two 4-bit unsigned inputs, A (a3, a2, a1, a0) and B (b3, b2, b1, b0), to generate an 8-bit product P (P7–P0).The multiplication process begins with the generation of partial products through bitwise AND operations between each bit of the multiplicand and the multiplier. For example, the first row of AND gates generates products such as (a0b0, a1b0, a2b0, a3b0), and similarly for other bits of B. These partial products are arranged in a diagonal or array form, representing the positional weighting of each bit in the final product.

The first column directly produces the least significant bit (LSB), P0 = a0b0, without any addition. The subsequent columns of partial products are summed using Half Adders (HAs) and Full Adders (FAs). Each adder cell combines two or three input bits, respectively, and produces a sum and a carry output. The carry outputs are propagated diagonally to the next column, while the sum outputs contribute to the corresponding bit position in the product.For instance, partial products like (a0b1, a1b0) are summed using a Half Adder to produce P1, and higher-order bits such as (a2b3, a3b2, carry bits) are combined using Full Adders to compute P6 and P7, the most significant bits (MSBs) of the final output. The diagonal arrangement of adders ensures regularity and ease of layout in both FPGA and ASIC implementations.This structure showcases the regular and modular architecture of the Braun multiplier, where each stage contributes systematically to the final 8-bit product. The simplicity of Half and Full Adder usage minimizes logic complexity, power consumption, and delay while maintaining accurate

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computation. Hence, this design is highly suitable for low-power digital applications requiring compact and efficient arithmetic hardware.
operation.

V.EXPERIMENTAL RESULT

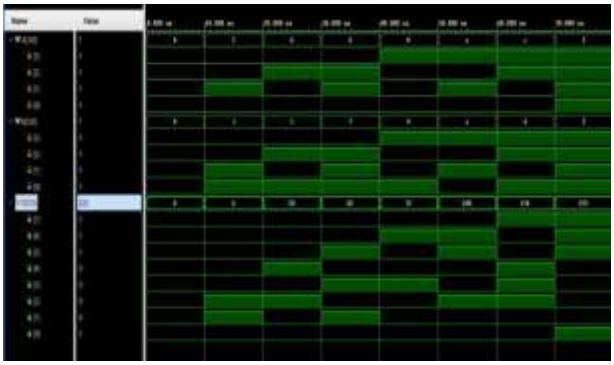

Fig 2. Simulation waveform of proposed method

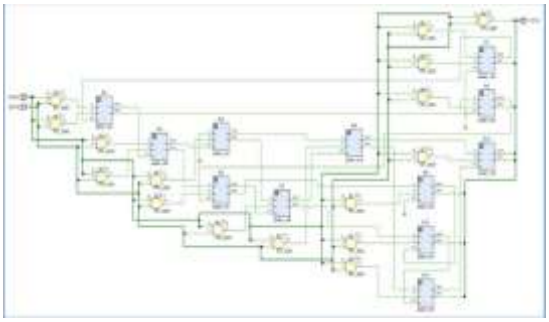

Fig 3.Schematic

Fig 4:Power report

VI.CONCLUSION

In conclusion, the 4×4 Braun Multiplier using Adder Cells was successfully designed, simulated, and synthesized on an FPGA platform, demonstrating both functional accuracy and hardware efficiency. The design effectively employs fundamental building blocks—Half Adders (HAs) and Full Adders (FAs)—to perform partial product addition in a systematic array structure. By using these simpler arithmetic units instead of complex and high-speed adders such as carry look-ahead or Kogge-Stone adders, the architecture achieves a balanced trade-off between speed, power consumption, and area utilization. This structural simplicity results in a highly modular design, making it easy to scale for higher bit-width multipliers such as 8×8, 16×16, or 32×32 by reusing the same basic cell layout.

The simulation results verified the functional correctness of the proposed design under multiple test conditions, confirming accurate multiplication outputs for all 4-bit input combinations. Post-synthesis analysis revealed that the design utilized only 15 Slice LUTs and 16 I/O pins, highlighting its exceptional area efficiency and low logic overhead. The power analysis conducted using Xilinx tools showed a total dynamic power consumption of 4.09 W, primarily due to I/O switching, while maintaining low static power and operating within a safe thermal envelope. The floorplanning and timing reports indicated that the design meets setup and hold timing constraints comfortably, ensuring reliable operation at moderate clock frequencies.

Furthermore, the compact layout and regular interconnection pattern of the Braun multiplier significantly simplify routing, placement, and verification during the FPGA synthesis process. This makes it highly suitable for low-power and resource-constrained environments, such as IoT devices, DSP modules, and portable embedded systems. The use of simple adder cells also enhances design portability, enabling implementation on various FPGA families or as a custom ASIC block with minimal redesign effort.

In summary, the proposed 4×4 Braun multiplier exhibits high accuracy, reduced power consumption, and excellent scalability, proving to be a robust and cost-effective solution for modern digital hardware applications. Its regular structure, predictable timing behavior, and low silicon footprint make it an ideal candidate for inclusion in VLSI arithmetic units, digital signal processors, image processing systems, and control applications where efficiency and reliability are critical. Future enhancements could involve incorporating pipeline stages for speed optimization, low-power logic techniques for energy efficiency, and hardware reuse methodologies for multi-bit multiplier architectures. Overall, this project reinforces the significance of simple, modular, and power-aware designs in advancing the field of digital arithmetic circuits.

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