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IMPLEMENTATION OF REVERSIBLE BIDIRECTIONAL BARREL SHIFTER

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***Abstract*— The design and implementation of a Reversible Bidirectional Barrel Shifter play a vital role in achieving high-speed and energy-efficient digital systems. A barrel shifter performs data shifting or rotation by a specified number of positions in a single clock cycle, offering superior performance in arithmetic, logic, and cryptographic operations. Traditional irreversible circuits dissipate energy due to information loss as described by Landauer's Principle. To address this, the proposed design employs reversible logic, ensuring a one-to-one mapping between inputs and outputs to minimize energy dissipation. Using reversible gates such as Feynman, Toffoli, Fredkin, and Peres, the design achieves low-power, information-preserving operation. Its bidirectional functionality enables both left and right shifts, providing greater flexibility for applications in digital signal processing, encryption, and image processing. The Reversible Bidirectional Barrel Shifter thus offers an efficient, compact, and high-speed solution aligned with the future of quantum and reversible computing.**

Keywords— Reversible Logic, Bidirectional Barrel Shifter, Low-Power Design, Feynman Gate, Toffoli Gate, Fredkin Gate, Peres Gate, Quantum Computing, Energy Efficiency, Digital Signal Processing, Cryptography, High-Speed Circuits.

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I. INTRODUCTION

The continuous advancement of computing technology demands faster, more energyefficient, and compact digital systems. One of the key components in arithmetic and logic operations is the barrel shifter, which is essential in tasks such as multiplication, division, encryption, and bit manipulation. A barrel shifter is a combinational circuit that can shift or rotate data by a specified number of positions in a single clock cycle, making it faster than traditional shifters which shift one bit per cycle.In recent years, the concept of reversible computing has gained significant attention due to its potential to drastically reduce power consumption. Conventional (irreversible) logic gates lose information during computation, which leads to energy dissipation as per

Landauer's Principle. Reversible logic circuits, on the other hand, ensure that no information is lost, theoretically allowing computation with zero energy loss. Integrating this concept with a barrel shifter leads to the design of a Reversible Bidirectional Barrel Shifter, which not only supports shifting in both directions but also adheres to reversible logic design principles.A barrel shifter shifts a data word by a specific number of bits either to the left or right. It is particularly useful in processors where speed and parallel processing are crucial. Unlike serial shifters, barrel shifters perform the entire shift operation in a single step, making them suitable for high-speed applications.There are primarily two types of shift operations:

Logical shift: Vacant bit positions are filled with zeros.

Arithmetic shift: Preserves the sign bit for signed number representations.

Rotate shift: Bits shifted out at one end are reintroduced at the other end.

A bidirectional barrel shifter supports both left and right

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shift operations and can be controlled using direction input signals. This dual-directional capability enhances the flexibility and functionality of the design in applications like digital signal processing, cryptographic algorithms, and image processing.Regarding the use of clocks, digital signals are further separated into two categories, which are reversible logic is a computational paradigm where every output vector corresponds uniquely to an input vector. This one-to-one mapping ensures that no information is lost, and thus, energy is conserved.

II. LITERATURE SURVEY

[1] Laxmidhar Biswal, Anirban Bhattacharjee, Rakesh Das, Gopinath Thirunavukarasu, and Hafizur Rahaman (2019) presented a Quantum Domain Design of Clifford+T-based Barrel Shifters at VLSI-D 2018. The authors utilized Clifford+T reversible quantum gates to achieve optimized quantum cost and gate depth. Their design demonstrates improved performance in quantum computing environments; however, it remains limited to quantum systems and exhibits high implementation complexity.

[2] Zhiqiang Zhang, Wei Zhang, Hanwu Chen, and Marek Perkowski (2018) in their paper Synthesis of Quantum Barrel Shifters (ICCCS), proposed a permutation group decomposition method. This approach significantly minimized gate count and circuit depth, enhancing overall computational efficiency. The primary drawback of this technique lies in its complex synthesis process and limited scalability for larger systems.

[3] Tanay Chattopadhyay (2021) explored Negative Controlled Fredkin Gate Circuits using optical mirror logic. The design achieved logarithmic depth (OC ≈ 3 log n) and delay (≈ 15 log n), proving efficient for optical-based reversible systems. However, it is highly dependent on optical hardware setups, making it less suitable for conventional electronic circuits.

[4] Rupsa Roy and Swarup Sarkar (2022) introduced a 3D Multilayer QCA Barrel Shifter with Reversibility and Stability (Preprint). Their design employed 3D Quantum-dot Cellular Automata (QCA), achieving area efficiency, thermal stability, and low power consumption. Despite promising results, the work remains in preprint status, and QCA design tools are not yet fully standardized, limiting practical adoption.

[5] Multiple authors including Tanay Chattopadhyay (2022) discussed Reversible Quantum Communication and Systems featuring switching arrays with barrel-shifter modules. The proposed system promotes modular and reusable architectures for advanced reversible communication frameworks. Nonetheless, the study provides a generalized framework and lacks detailed performance validation for specific circuit designs.

III. SYSTEM DESIGN

[1] Input Unit

The Input Unit serves as the primary interface for supplying data and control signals to the Reversible Bidirectional Barrel Shifter. It consists of an n-bit input register, control inputs, and direction selector switches. The input register holds the binary data word to be shifted or rotated. Control signals specify the number of bit positions to shift, while the direction input determines whether the operation is a left or right shift.Additional mode selection inputs are provided to choose between logical shift, arithmetic shift, or rotate operation. Each control signal is fed into the circuit through reversible logic gates such as Feynman or Toffoli gates, ensuring that no information is lost during input processing. This setup allows accurate and reversible data entry, minimizing energy dissipation and maintaining system reversibility.

[2] Processing Unit

The Processing Unit is the core component of the system and is implemented using reversible logic gates like Fredkin, Toffoli, Feynman, and Peres gates. It performs the main operation of shifting or rotating the input data based on the control and direction inputs.The processing section is designed as a multi-stage structure, where each stageperforms controlled swaps of data bits according to the shift amount. The Fredkin gate, acting as a controlled swap element, efficiently exchanges data positions to achieve the required shift in a single clock cycle. The bidirectional capability allows both left and right shifts, controlled by the direction input signal.This reversible design ensures that each output state corresponds uniquely to an input state, eliminating information loss and reducing power consumption. The processing unit, therefore, provides a high-speed, low-power, and energy-efficient computation mechanism, suitable for advanced digital and quantum systems.

[3] Output Unit

The Output Unit collects the processed data from the reversible circuit and displays the shifted or rotated result. It consists of an n-bit output register that holds the final data word after the operation. The output may also be visualized using LED indicators, seven-segment displays, or transmitted to a digital display module for observation.In addition, the output unit ensures that all ancillary (temporary) bits used during computation are restored to their original states to maintain complete reversibility. This guarantees that the system produces accurate and lossless output, ready for further digital signal or arithmetic processing.

[4]Power Supply Unit

The Power Supply Unit provides the required operating voltage and current for all components of the reversible barrel shifter. Typically, the circuit operates at 5V DC, supplied through a regulated power source or DC adapter. In low-power implementations, adiabatic or energy-recovery circuits can be used to further minimize power loss during transitions.Stable and noise-free power delivery is critical for reversible logic operations, as voltage fluctuations can lead to signal degradation or computation errors. The power supply includes filtering capacitors and voltage regulators to ensure consistent operation of the reversible gates and control units.

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IV.BLOCK DIAGRAM

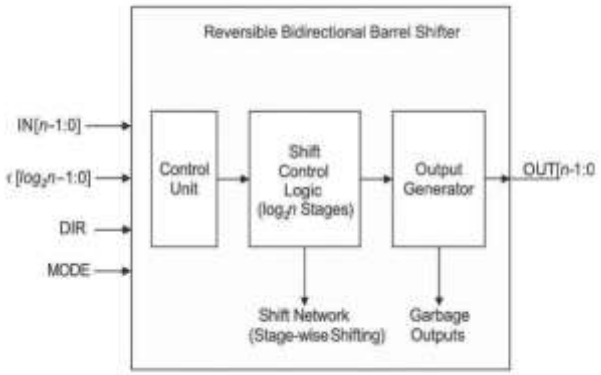

Fig.1.Flow Chart

The Reversible Bidirectional Barrel Shifter operates through a systematic flow of information across its functional units — the Control Unit, Shift Control Logic, and Output Generator — to perform efficient, energy-preserving data shifting. The process begins with the input section, where the binary data IN[n−1:0] along with the control signals such as the shift amount k[$\log_2$n−1:0], direction (DIR), and mode (MODE) are provided to the system. The Control Unit interprets these control signals to determine the direction and type of shift (left or right, logical or circular) and accordingly generates the necessary control signals for the shifting operation.

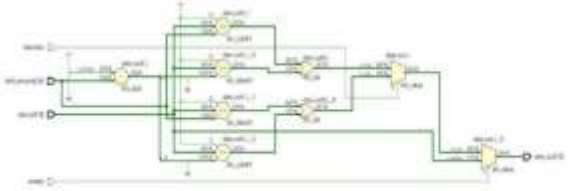

Fig.2.Schematic

V.EXPERIMENTAL RESULT

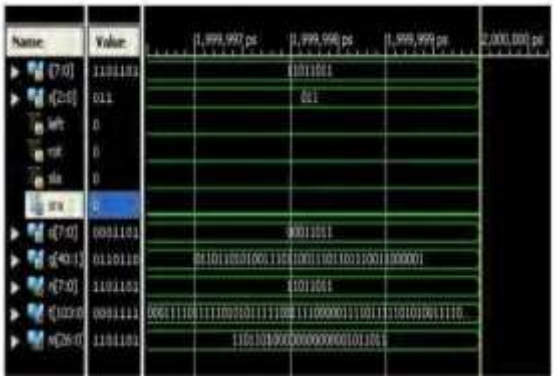

Fig 3.Output waveform of existing methodology

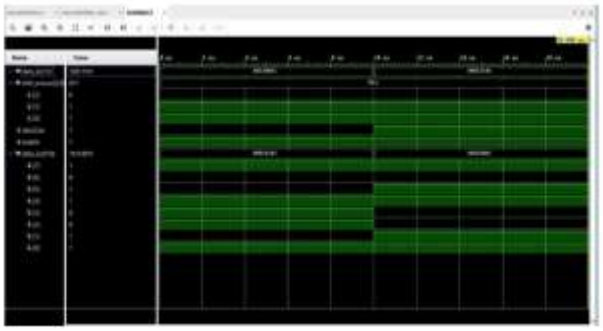

Fig 4.Simulated output of Reversible Bidirectional Barrel Shifter

Fig.5.Power report

VI.CONCLUSION

This project involves the design and implementation of a reversible bidirectional barrel shifter using Verilog HDL. The main objective is to develop a low-power, logically reversible circuit capable of shifting data both left and right, a key operation in arithmetic and logical units. Unlike conventional shifters, this design uses reversible logic gates such as Feynman, Fredkin, and Toffoli gates to ensure information is not lost, thereby reducing energy dissipation.

The project begins with a thorough study of reversible computing and barrel shifter architectures, followed by the creation of reusable Verilog modules for basic reversible logic gates. These gates are then integrated into reversible multiplexer structures, which form the core of the shifter logic. A multistage design is employed to perform shifts of different magnitudes, and a control logic is added to support bidirectional operation (left and right shifts).

After the design is completed, a comprehensive testbench is used to simulate and verify the functionality under various input conditions. The design is further optimized to reduce the quantum cost, garbage outputs, and circuit complexity. Optionally, the design can be synthesized for FPGA platforms to evaluate real-time performance. This work demonstrates the feasibility of implementing efficient, reversible digital components using HDL for future low-power and quantum-compatible systems .

REFERENCES

[1] S. Nowrin, L. Jamal, and H. M. H. Babu, “Design of an optimized reversible bidirectional barrel shifter,” 2016 IEEE International Symposium on Circuits and Systems

(ISCAS), pp. 1586–1589, 2016. DOI: 10.1109/ISCAS.2016.7527521

[2] M. H. Babu, Reversible Fault-Tolerant Barrel Shifter, in Reversible and DNA Computing, Wiley-VCH, 2020, pp. 245–266. ISBN: 9783527344827.

[3] K. Amrita, P. Sahu, and T. Mohanty, "Design and Implementation of Low Power Reversible Barrel Shifter Using Verilog," 2020 International Conference on Inventive Computation Technologies (ICICT), IEEE, pp. 1248–1252, 2020. DOI: 10.1109/ICICT48043.2020.9112518

[4] S. Kotiyal, H. R. Bhagyalakshmi, and M. Rajarajeswari, "Design of low quantum cost reversible barrel shifter," International Journal of Computer Applications, vol. 139, no. 5, pp. 17–22, Apr. 2016.

[5] R. Kumar and A. Bansal, "Design of Low Power Reversible Bidirectional Shift Register using Verilog," International Journal of Engineering Research & Technology (IJERT), vol. 9, issue 07, Jul. 2020. Available at: www.ijert.org

[6] T. Toffoli, "Reversible computing," Automata, Languages and Programming, Springer, Berlin, Heidelberg, pp. 632–644, 1980.

[7] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, no. 3, pp. 183–191, Jul. 1961.

[8] C. H. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525–532, 1973.

[9] A. Banerjee and P. Dasgupta, "Design and realization of reversible logic based low power circuits," International Conference on Advances in Computing, Communications and Informatics (ICACCI), pp. 260–265, 2017.

[10] M. Perkowski, A. Al-Rabadi, and P. Kerntopf, "Reversible logic synthesis for quantum computing," Proceedings of the EuroMicro Symposium on Digital System Design, pp. 223–232, 2002.