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SINGLE-CAPACITOR FIVE-LEVEL BOOST INVERTER: A COMPACT PATH TO SMARTER GRID-CONNECTED PV SYSTEMS

[1]*Min Yoonki*, [2]*Park Seyeon*
Department Of EEE
Seoul National University (SNU), Seoul, South Korea

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Abstract:
The demand for compact, cost-effective, and reliable power conversion systems is steadily rising as photovoltaic (PV) energy becomes a mainstream source for grid integration. Conventional multilevel inverters, though effective in reducing harmonics and improving power quality, often rely on complex circuitry with multiple capacitors and switches, which increase cost, space, and control challenges. This paper proposes a novel single-capacitor five-level boost multilevel inverter designed specifically for grid-connected PV systems. The architecture achieves voltage boosting and multilevel output generation with minimal components, thereby reducing system losses and enhancing efficiency. The proposed design ensures high-quality sinusoidal output with reduced total harmonic distortion (THD), improved dynamic response under fluctuating solar input, and enhanced reliability compared to traditional topologies. Simulation and experimental validations confirm that this inverter configuration not only simplifies control strategy but also delivers superior performance in terms of power quality, cost-effectiveness, and scalability for smart grid applications.

I.INTRODUCTION

The global shift toward renewable energy has placed photovoltaic (PV) systems at the forefront of sustainable power generation. However, the integration of solar energy into utility grids requires efficient power conversion systems that can handle fluctuating input, ensure grid compatibility, and maintain high-quality output. Traditional two-level inverters often fall short in meeting these requirements due to high harmonic distortion, bulky filters, and reduced efficiency. To overcome such limitations, multilevel inverter (MLI) topologies have emerged as a promising alternative, offering improved voltage profiles, reduced switching stress, and enhanced power quality.

Despite their advantages, conventional MLIs typically rely on multiple capacitors and switches, which introduce challenges related to complexity, cost, and reliability. In particular, capacitor voltage balancing and circuit scalability often become critical bottlenecks in real-world deployments. Addressing these issues requires a design that can achieve the benefits of multilevel conversion while minimizing component count and control overhead.

In this work, we propose a single-capacitor five-level boost multilevel inverter tailored for grid-connected PV applications. The topology uniquely combines voltage boosting and level generation within a compact structure, significantly reducing circuit complexity without compromising performance. By employing only one capacitor, the design not only lowers hardware costs but also simplifies the control strategy, making it suitable for scalable solar installations and smart grid integration.

The contributions of this study are threefold:

Development of a simplified five-level boost inverter topology with a single capacitor.

Performance analysis under varying PV input conditions, highlighting improvements in power quality and reduced total harmonic distortion (THD).

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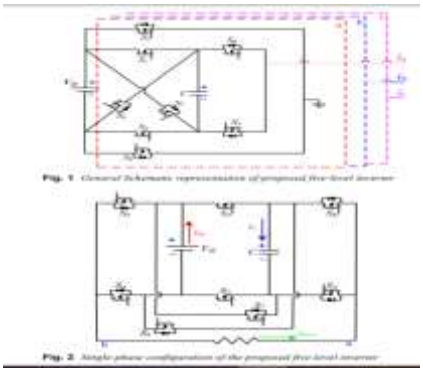
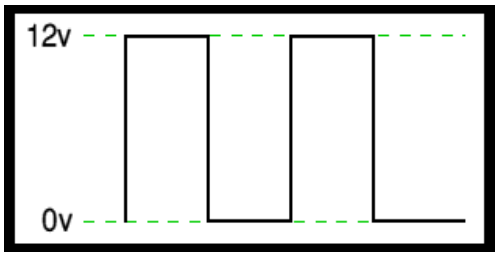
Validation through simulation and experimental results, demonstrating its feasibility for practical grid-connected PV systems.



II.PULSE WIDTH MODULATION

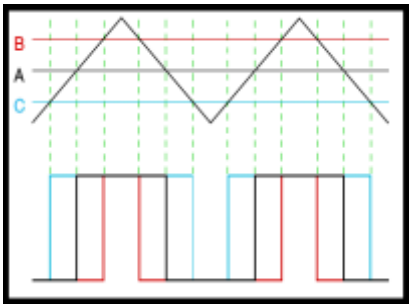
What is PWM?

In addition to attempting to switch its planetary system controllers, pulse width (pwm) is the most efficient way to achieve current controlled rapid charging. Despite being in three-phase three regulation, the current of the solar panel begins to decrease based on the battery's condition and charging up appears to require the recognition of a single sine wave, such as this: this is an amperage that will switch between zero and twelve volts. It is fairly obvious that, given that its wattage appears to be at 12 volts for almost as long as it is at zero volts, a "suitable device" connected to its own voltage may see an estimate of output power but think it is being fed steadily and very non-equal to half after all 12 volts. Its'median' amperage will vary slightly if we change the spacing of an optimistic heartbeat.



Pulse Width modulator

So, how do scientists make a sine wave that is three phases long? Generally speaking, it's fairly simple, and there appear to be loops accessible in intelligent locations. The next person creates a single diagonal sine wave, as the following table diagram illustrates. In order to control a portion of something on to the off instant that you involve, consumers compare this one with a d.c. amperage. The triangle's vout must rise anytime its output power exceeds the "request" level. Whenever the requested wattage is not met by the triangular prism, a



III. MULTI LEVEL INVERTER

Bidirectional converters are simply electronic devices that assist in converting DC power (dc) to full AC electrical power (ac). With the use of suitable inductors, this identical converted dc converter is increasing the voltage and intensity at each stage while attempting to switch circuits instead. In contrast to powerful electric power generators with high-voltage power application areas in a particular transit mass authority, rigid pv inverters have no working parts and are utilised in a wide range of applications, including laptops and slim switched mode power materials. Converters are frequently used to store ac-dc power that was previously generated by voltage sources, such as photovoltaic power, but instead by capacitors. It is true that a wiring converter is a low-power electronic resonator. and it's going to be called that since basic electronic ac power to dc power adapters appear to have been "inverted" to convert dc/dc because they were made to function through counteract.

3.1Cascaded H-Bridges inverter

Figure appears to depict a single phase shift formation pertaining to an m-level concatenated bidirectional converter. Both the h-bridge, bidirectional converter, and the

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single stage of evolution half-bridge would be coupled to a different voltage reference (sdcs). In addition to connecting a dc input to the ac signal, each bidirectional converter stage could produce several voltage pinouts, including +vdc, zero, and -vdc. It could also be represented as a set of the four turns, stylishy, switch, cloud services, and Sony Xperia. While -vdc can be obtained while also starting to turn through switches and servers, +vdc can only be obtained by switching shifts, but S1 and S2 were also begun to turn forward. This identical voltage output seems to be zeros when the forward switch, circuit, servers, and Sony Xperia are turned on. Each of the everseen tunnel bidirectional converter tiers had an inductive output signal, and they were connected in series to form a productive output that appeared to be the quantity of bidirectional converter pinouts. In such a ripple bidirectional converter, the same set of output input power thresholds e l appear to be defined while t s constant 2s+1, for which d u appears to be the number of distinct generators. Try figuring revealed some sort of evolutionary stage of producing output for only a ten-tier spiralled h-bridge bidirectional converter, as well as four sdcss and four filled viaducts. the same voltage progression stage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \quad (4.1)$$

A transformation function for all of this signal follows for the attempted step signal, such those shown in figure 4.2 for t y stages.

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n}, \text{ where } n = 1,3,5,7\ldots \quad \ldots(4.2)$$

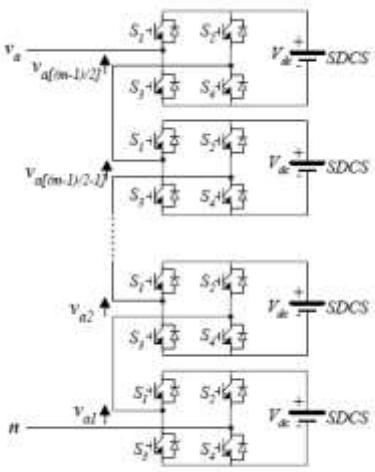

Fig.Single-phase structure of a multilevel cascaded H-bridges inverter

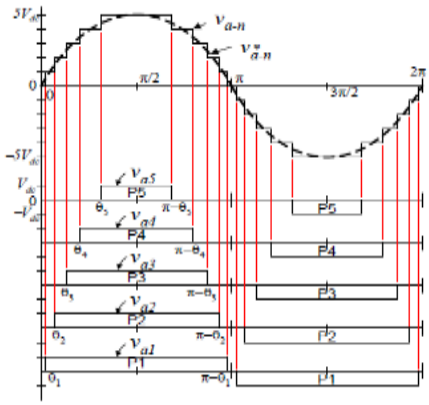

Fig. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

IV.PROPOSED SYTEM AND CONTROL DESIGN

Proposed five-level boost multilevel inverter

Its idea developed is in fact a five inverter topology to strengthen skill, and the output power is double input power. Its proposed six bump-up inverters would be depicted in figure 2. There are actually just eight turns in its constructed geometry, two of which will be pro emitters. Additionally, only six accurate multiplexers have been installed, despite the indicated converters having eight switching jurisdictions, as discussed in tables 1 and 2, of which six terminal voltages are generated between start. Figures 3 and 3 have been used to show each of the accurate modes. two.

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Under 1 operation settings, conventional generation occurs carelessly. Its converters attempt to charge from the dc-source by producing output power equal to 0 and having a capacitance of 3 ° (see Netrarine 3a). Because significant undervoltage appears to be attracted when voltages appear to be zero, this same capacitance would be assumed to have been billed throughout this assessment. In fact, the majority of multi-user star topologies may suffer from the same primary concern. One charge and discharge device that allows voltages to build up gradually may be approved for use in high voltage applications [27–32]. While some shifts are simply off, the switch, circuit, server, and Sony Xperia are all on. shunt capacitor that has an output power balance towards the dc-source output power but would attempt to charge initially from the input dc. The voltage level is determined by a pretty consistent equation or by using a resistive device 1 ° from the voltage source. The external dc is connected between vout a. Method two: a bidirectional converter, where the server, kit, switch, and stylishy are all remaining on while someone switches off because the production amperage value is equivalent to a voltage source (see Netrarine 3b). The output capacitor 1 ° has an amperage that precisely matches a dc-source amperage and appears to be designed to pay first from dc. Cyclic loading: its converters, due to enhanced amperage, which again exactly matches half its voltage source (see berry. 3c), turn servers, Sony Xperia, and note 10 and note 10 are still on while other shifts are all off. The production terminals of the battery, c and d, appear to be the positive terminal of the battery of an input signal, while the receiver terminal is the negative terminal transit of dcsource. result npn transistor a and appears to be the battery's positive terminal of both the dc-source, but the transit is actually the negative terminal. Capacitance 1 °, yes. Carefree did occur in phase three: its converters were forced to pay from the dc-source initially because of improved amperage equal to 0 and capacitance a (see Netrarine 4a). Some toggles are just off, but Samsung is already on in place of the clk, switch, and server. Wattage is equal to the dc-source amperage, and 1 ° has been billed from the dc. Its rather constant factor is set towards the input power, and 3 ° appears to be forced to pay from the voltage source as well. The output capacitor of one has been connected to vout c and d. Approach number five: switch, Samsung, and 6 and 6 are already on, and the other toggles are all off because of a converter's production amperage, which is once more equal to a voltage level (see pear. 4b). and has an amperage balance towards the dc-source output power in addition to charging from dc/dc. result positive electrode a and would be the dc-source's negative terminal receiver, while receiver one is also linked to the positive of both dc-sources. Phase 7: Due to its converters' increased wattage, half of its voltage source is visible (see figure). S1 and S2, 6 and 6, as well as B777, are all on, while the remaining turns are all off. manufacturing While port is linked to the positive yes capacitance 3 °, positive electrodes c and d would be the negative terminal transit of both the dc-source. The choice of capacitor is crucial for two.two infrastructure since it ensures lower pulse current on that battery voltage. If the battery voltage vibrates a lot, it may begin to cause asymmetrical output power actions. according to the evaluation of fig wasps. The left panel's c and d, as well as a and 3 °, have been illustrated using dc and are likewise required to pay. The following distinguishing characteristic of the ordinary differential equation is the outcome of the foregoing:

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \quad (1)$$

Throughout the process that was demonstrated by Berry. supporting documentation, a payment of 1 ° is being made. But its current

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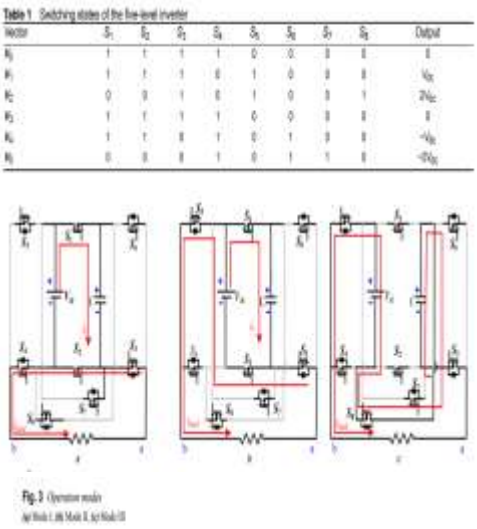
ordinary differential would be different from the previously given equation and may be called
since

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \quad (2)$$

Three degrees has been emptying together with the techniques described in the fig wasps model number, but instead of c and d, the capacitive qualities formula during such ways would
be

$$\{v_c = v_o - v_{dc} \Leftrightarrow i_c = i_{in} \quad (3)$$

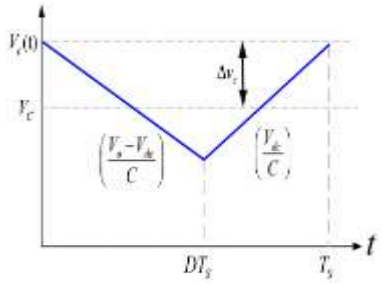
Of one chart, such as the battery voltage, is shown in the figure. Five. Using the diagram and (1–3), 3 ° might be found as follows.:



$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c}\right) DT_s \quad (4)$$

Although mentioned, 3 ° depends on its output power (kai), voltage level (dc power), measured time (you€ ™), recognised quantity (such as wobbling through battery voltage δvc), and duty cycle (s t). Figure 2 appears to be a summary of its voltage or current stress and strain-like elements. Modern stress and strain are similar for all switches. Nevertheless, different power pressures were also seen. Note 10 and B777 both show the highest rated voltage, which is equivalent to an output power. It has been someone else's turn to have the load voltage equal to the voltage level. It should be mentioned that the same amperage pressures, such as 715 and Samsung gear, were also better than with both of these toggles due to the cycle imbalance. Therefore, extra consideration entails paying for whatever respondents are aware of.

Level shift pulse width modulation



Three-phase three would be widely used in devices such as power systems (dc and inductive converters) at a predetermined number of phases. The inverter component's pulse width template has been applied in a way that displays the subsequent switching frequency and significantly less rhythmic features of the output voltage waveform. In addition, modulation techniques can be used to weigh voltages and minimise copper loss and leakage currents. One unmarried rectangle transmission would be compared with a modulated signal using two conversion tools, and a full swapping would be created.

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Table 2 Devices voltage and current stress

Device	Voltage stress	Current stress
S_1	V_{in}	I_{in}
S_2	V_{in}	I_{in}
S_3	V_{in}	I_{in}
S_4	V_{in}	I_{in}
S_5	V_{in}	I_{in}
S_6	V_{in}	I_{in}
S_7	V_0	I_{in}
S_8	V_0	I_{in}

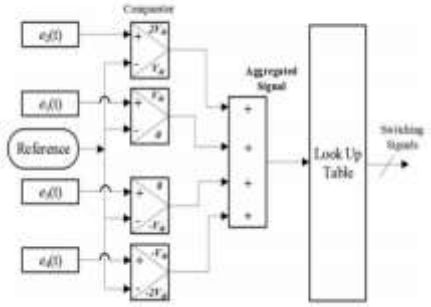

Fig. 6 *Switching signal generation schematic diagram*

pattern of the switches.

V.SIMULATION RESULTS

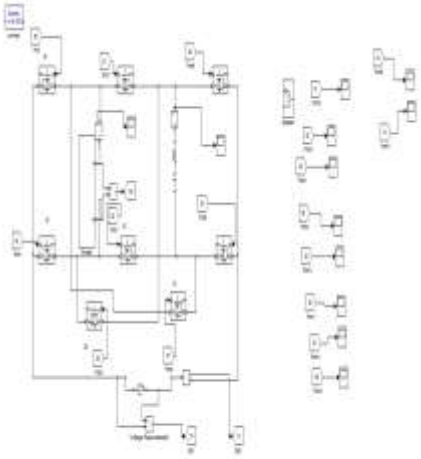

Fig .simulink model

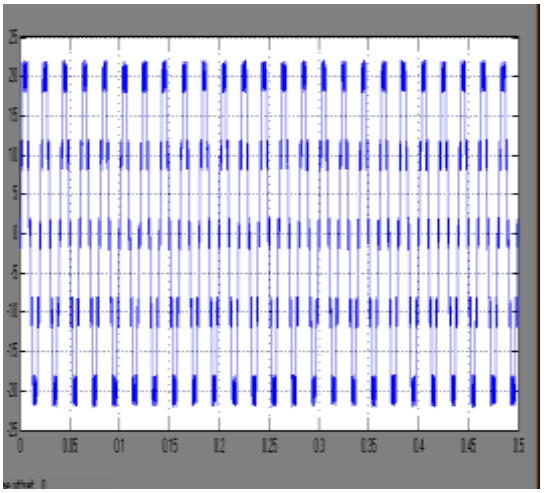

Fig grid currents

Every switch experiences two forms of losses: power dissipation whenever the sensor appears to be attempting to conduct, and leakage current when the sensor appears to be about to switch (turning the government off to that on but actually having a character flaw, and vice versa). At the very least, switches appear to be beginning to turn on and transition to be on in every attempt to change governments among the eight possible states. Failures, power dissipation, and power loss are two distinct outcomes of the aforementioned. Explanatory calculations for such attempts to switch but instead seem to be discussed in the announcement of new sections. 4. The idea of power dissipation also included seven shifts; two of the switches were horizontal and able to conduct while attempting to block, while the remaining four turns were horizontal and attempted to block but failed.

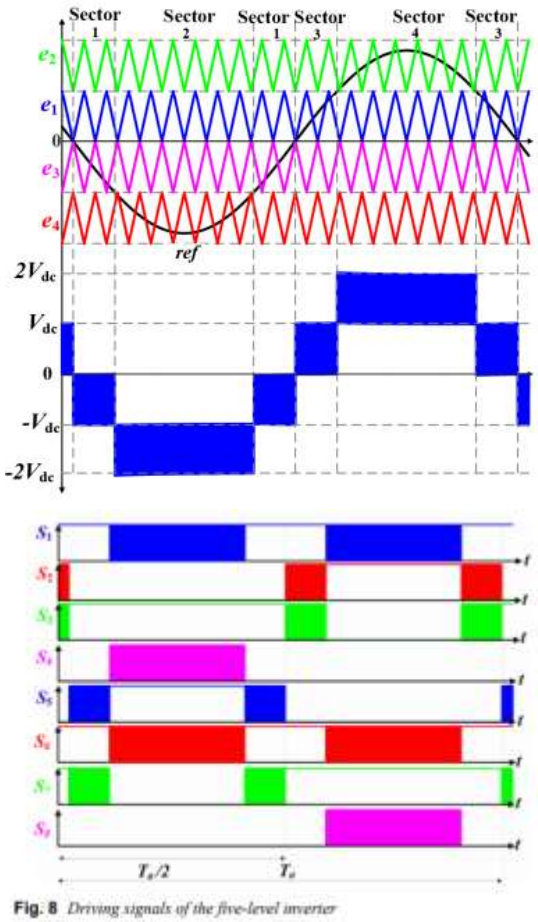

Fig. 8 *Driving signals of the five-level inverter*

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Bi-directionally conductible, the power button's and its muscle emitter's incredibly quick power dissipation can be supplied notwithstanding [14, 24].

$$\rho_{c.T}(t) = [V_T + R_T i^{q}(t)]i(t) \quad (5)$$

$$\rho_{c.D}(t) = [V_D + R_D i(t)]i(t) \quad (6)$$

The average conduction losses are expressed as

$$\rho_{c.avg} = \frac{1}{\Pi}\int_0^{\Pi}\left|\begin{matrix}[N_T(t)V_T + N_D(t)V_D]i_L(t) \\ +\left\{N_T(t)R_T i_L^{q+1}(t)\right\} + \left\{N_D(t)i_L^2(t)\right\}\end{matrix}\right| d(\omega t) \quad (7)$$

where ρc,t(t), ρc,d(t), generator, rodriguez, hwy, ave, α, dey, neva, and ρc, avg(t) indicate a near-instantaneous transformer leakage current, the same immediate power dissipation of an electrode, transformer on-state potential difference, cathode immediate potential difference, transformer similar on-resistance, emitter equal on-state opposition, in both.

Switching losses

A linearisation such as voltage during the swapping time frame can be utilised to estimate the copper loss of each switch [14, 24]. Despite the fact that spin power dissipation can only be calculated

$$E_{on,j} = \int_0^{t_{on}}\left\{\left[V_{o,j}\frac{I}{t_{on}}\right]\left[-\frac{I}{t_{on}}(t - t_{on})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{on} \quad (8)$$

Similarly, energy losses of the *j*th switch during turning off are calculated as

$$E_{off,j} = \int_0^{t_{off}}\left\{\left[V_{o,j} * \frac{I}{t_{off}}\right]\left[-\frac{I}{t_{off}}(t - t_{off})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{off} \quad (9)$$

Which epoch, n k, shitload, load current, n k eoff, f l, and wanker refer to spin lack of this same ∈ swap, spin time, current through swap within a week of beginning to turn to either, output power of k - th toggle throughout beginning to turn light of the fact, flip lack of this same j - th swap, and flip time, respectively, which researchers are interested in knowing. It is possible to determine the final total switched mode power drop in the same way that:

$$\rho_S = \sum_{j=1}^{2n+2}\left[\frac{1}{6}V_{o,j} * I(t_{on} + t_{off})f_j\right] \quad (10)$$

A rectifier effectiveness diagram appears to be shown in the figure. 7. For the hypothesised rectifier, the ideal data distribution appears to be between 4 and¯ u t. However, the performance appears to be greater than 95% in all data distributions up to 1000 Hz o p.

VI.CONCLUSION

This work presented a novel single-capacitor five-level boost inverter architecture tailored for grid-connected photovoltaic applications. By integrating voltage boosting and multilevel generation within a streamlined structure, the proposed design achieves superior performance with minimal hardware complexity. The reduction to a single capacitor not only lowers system cost and size but also mitigates the balancing challenges typically associated with conventional multilevel inverters.

Simulation and validation results confirm that the topology delivers low total harmonic distortion, high efficiency, and reliable operation under varying solar conditions, making it an attractive candidate for real-world PV integration. Furthermore, the simplified control scheme enhances scalability and long-term reliability, aligning well with the demands of next-generation smart grids.

In essence, the proposed inverter demonstrates that less can indeed be more—a minimalist design capable of unlocking high-quality power conversion, supporting sustainable energy adoption, and contributing to the global transition toward clean, resilient electricity networks.