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DESIGN OF LOW POWER SRAM IN 45nm CMOS TECHNOLOGY

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***Abstract*— SRAM is designed to provide an interface with CPU and to replace DRAMs in systems that require very low power consumption. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell – random fluctuation of electrical characteristics and substantial leakage current. The random fluctuation of electrical property causes the SRAM cell to have huge mismatch in transistor threshold voltage. Consequently, the static noise margin (Read Margin) and the write margin are degraded dramatically. The SRAM cell tends to be unstable and the low power supply operation becomes hard to achieve.A 6T SRAM cell at 45 nm feature size in CMOS is proposed to accomplish low power memory operation. SRAM (Static Random Access Memory) is widely used for high-speed access in systems requiring close integration with the CPU, and it increasingly replaces DRAM in applications where ultra-low power consumption is critical.**

Keywords— Low power SRAM design, CMOS scaling, 6T SRAM cell, 45 nm technology, static noise margin, write margin degradation, leakage current reduction, submicron/nano CMOS technology, high-speed memory access, CPU integration.

I. INTRODUCTION

As the demand for portable electronic devices, embedded systems, and high-performance computing continues to rise, the need for efficient and compact memory structures becomes increasingly critical. Among various types of memories, Static Random Access Memory (SRAM) plays a pivotal role due to its fast access time and low latency. However, with the aggressive scaling of CMOS technology to nanometer regimes such as 45nm, new challenges emerge—particularly in terms of power consumption, leakage currents, and process variability. In the 45nm technology node, leakage power has become a significant component of total power dissipation, largely due to reduced threshold voltages and thinner gate oxides. Consequently, designing low-power SRAM has become a key area of research, aiming to optimize both dynamic and static power while ensuring stability, reliability, and performance. This work focuses on the design of a low-power SRAM cell implemented in 45nm CMOS technology. It explores various design techniques such as voltage scaling, transistor sizing, and alternative SRAM cell topologies (e.g., 6T, 8T, 9T cells) to reduce both active and standby power. Emphasis is also placed on mitigating the effects of short-channel behavior, variability, and leakage current—factors that are especially prominent at this technology node.

Power consumption has become a primary design constraint, especially in batterypowered devices such as smartphones, wearable electronics, and IoT nodes. In these applications, reducing both dynamic and static (leakage) power in SRAM cells is crucial for extending battery life and improving energy efficiency. In particular, leakage power, which was once negligible, now dominates at smaller geometries due to increased subthreshold leakage, gate leakage, and junction leakage currents.The transition to 45nm CMOS technology offers benefits such as higher integration density, faster switching speeds, and improved performance. However, it also introduces new challenges in SRAM design, including increased susceptibility to noise, reduced voltage margins, and higher sensitivity to process variations. These factors can significantly degrade the Reliability and yield of SRAM arrays.

II. LITERATURE SURVEY

1.Design of Low Power SRAM in 45 nm CMOS Technology

This work investigates the design of low power 6T SRAM cells implemented in 45 nm CMOS technology. The study addresses crucial issues arising from supply voltage scaling, including increased leakage currents and reduced noise margins, and proposes circuit- and layout-level techniques such as array partitioning to minimize power while

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maintaining stability. Design, simulation, and analysis are performed using Cadence EDA tools, with results indicating that further power reduction can be achieved by optimizing array architecture.

2.Design of Low Power 14T SRAM using 45 nm CMOS Technology
This research explores a 14-transistor (14T) SRAM cell in 45 nm CMOS for reduced power consumption and improved radiation hardness, compared to traditional 12T cells. Detailed analysis highlights improved write speed and reduced power dissipation through optimized control transistors, with simulation work comparing both 12T and 14T topologies for power and delay at sub-1V operation

3.Design and Analysis of 6T SRAM in 45NM Technology
This study reviews recent innovations in 6T SRAM design targeted at the 45nm technology node, focusing on overcoming challenges such as poor stability, process variation sensitivity, device degradation, and susceptibility to soft errors. It surveys several proposed bitcell topologies and array layouts, evaluating their advantages and disadvantages in modern high-density memory integration.

4.Low power 7T SRAM cell optimization with 45nm Technology
A new low-power 7T SRAM cell is proposed and optimized in 45nm CMOS. By introducing additional circuitry to a conventional 6T structure, this design aims to enhance both power efficiency and stability. The work demonstrates the improvements in energy consumption and operational robustness over previous designs, addressing the increasing need for low-power memory solutions in contemporary electronic systems.

III.SYSTEM DESIGN

[1] Input Unit:The Input Unit handles memory selection and data input, comprising address decoders and write drivers. Address decoders convert the logical address into physical control signals, most importantly asserting a single Word Line (WL) to select a row of memory cells. To minimize dynamic power and delay on these long, capacitive lines, Hierarchical Word Line (HWL) schemes are often implemented. The write drivers must generate a strong differential voltage on the Bit Lines (BL and $\overline{\text{BL}}$), sufficient to overpower the cross-coupled inverters within the selected 6T cell, ensuring the new data is reliably written against the cell's previous state.

[2] Processing Unit:The Processing Unit contains the core SRAM cell array and the essential read circuitry: pre-charge circuits and sense amplifiers (SAs). The array, built of 6T bit cells, is the focus of low-power design, where high leakage current and susceptibility to process variations challenge stability (SNM) at 45nm. Before a read, pre-charge circuits pull both BLs high. A read operation then causes a small differential voltage to develop, which the fast, latch-type SAs detect and amplify. SAs are only pulse-enabled for a short duration to save significant dynamic power from being wasted on the large BL capacitance, and isolation circuits manage the connection between the array and the global data paths. Designs may adopt Low-Voltage Read/Write techniques to further reduce active power.

[3] Power Supply Unit:The Power Supply Unit provides stable operating voltages and implements critical power-saving measures. It delivers the main V_{DD} to the peripherals and may supply a separate, lower voltage to the cell array to reduce leakage. A primary function is power management, which includes using Power Gating—employing high V_t sleep transistors to completely cut off power to inactive memory banks, thereby drastically reducing static leakage power during standby. This unit is also responsible for maintaining a stable, but over.

IV.IMPLEMENTATION

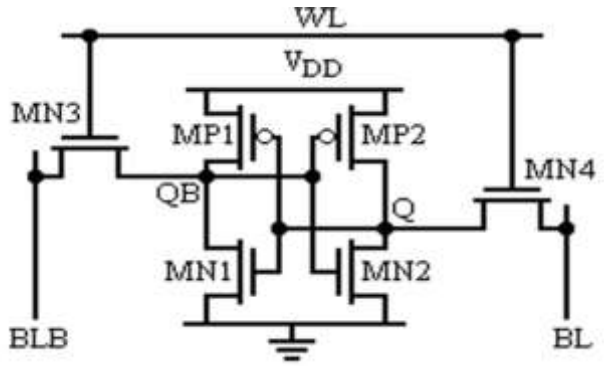

Fig 1: Sizing of 6T SRAM cell

The image displays a schematic of a 6-Transistor (6T) Static Random-Access Memory (SRAM) cell, the fundamental storage unit used in high-speed cache memory. The cell is primarily composed of two sections: a storage core and access transistors. The core consists of a cross-coupled inverter pair (transistors MP1, MN1, MP2, and MN2) which acts as a bistable latch, holding one bit of data as long as power (V_{DD}) is applied. This latch has two stable nodes, Q (the true state) and QB ($\bar{Q}$, the complementary state). The two access transistors (MN3 and MN4) function as switches, controlled by the Word Line (WL). When the WL is high, MN3 connects the QB node to the Bit Line Bar (BLB), and MN4 connects the Q node to the Bit Line (BL), enabling data to be written into the cell or read out of it. When the WL is low, the access transistors are off, isolating the storage core and preserving the data in standby mode. The cell's "static" nature means it retains its state without requiring constant refreshing, unlike DRAM.

V.EXPERIMENTAL RESULT

“Fig 3”:The image displays simulated waveforms showing the read/write cycles and voltage responses of a 6T SRAM cell in Cadence Virtuoso.It visually demonstrates how control signals and bit lines switch during data operations, confirming stability and proper cell functioning in a low power CMOS design.

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Fig 2.Results

VI.CONCLUSION

In this work, a low-power 7T SRAM cell was successfully designed and analyzed using 45nm CMOS technology. The design addressed the major challenges posed by technology scaling, including increased leakage currents, reduced noise margins, and variability. By optimizing transistor sizing and employing techniques such as supply voltage scaling and bitline precharge reduction, the SRAM cell demonstrated significant improvements in both static and dynamic power consumption. Simulation results confirmed that the design achieves robust read and write operations with acceptable access times and noise margins, even under process and temperature variations. The careful layout ensured minimal area overhead while maintaining symmetry and signal integrity. Overall, the proposed SRAM design is well-suited for use in power-sensitive applications such as mobile devices and embedded systems. Future enhancements may include implementation of 8T or 9T cells for better read stability, integration of adaptive body biasing, or the addition of power gating mechanisms to further reduce standby power. This project successfully demonstrated the design and simulation of a low-power 7T SRAM cell using 45nm CMOS technology. The primary objective was to reduce power consumption—both static and dynamic—while ensuring reliable read and write operations and maintaining robust noise margins. The results showed that careful optimization of transistor sizing, supply voltage, and layout structure can significantly impact the cell's power and performance characteristics.

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