International Journal of
DATA SCIENCE AND IOT MANAGEMENT SYSTEM
ISSN: 3068-272X www.ijdim.com Original Research Paper

ENERGY-EFFICIENT VLSI ARCHITECTURE FOR RECONFIGURABLE FIR FILTERS USING OPTIMIZED CARRY BYPASS ADDERS

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Abstract

The growing demand for high-performance digital signal processing (DSP) systems in wireless communication, multimedia processing, biomedical instrumentation, and embedded applications has increased the need for energy-efficient and reconfigurable hardware architectures. Finite Impulse Response (FIR) filters are fundamental components in DSP systems due to their inherent stability, linear phase characteristics, and adaptability to various signal processing tasks. However, conventional FIR filter implementations often suffer from increased power consumption, larger silicon area, and higher computational delay, particularly when operating at high sampling rates. This paper presents an energy-efficient VLSI architecture for reconfigurable FIR filters using optimized Carry Bypass Adders (CBAs). The proposed architecture integrates reconfigurable filter structures with an enhanced carry bypass adder design to improve arithmetic processing efficiency while reducing propagation delay and switching power consumption. The optimized CBA enables faster carry propagation through strategically designed bypass paths, thereby minimizing critical path delay and improving overall filter performance. Furthermore, the reconfigurable architecture supports dynamic coefficient updates and adaptable filter orders, making it suitable for multi-standard and adaptive signal processing applications. The design is modeled and evaluated using hardware description language (HDL)-based implementation and synthesized on a modern VLSI platform. Performance metrics including power consumption, area utilization, operating frequency, and processing delay are analyzed and compared with conventional FIR filter architectures. Experimental results demonstrate that the proposed approach achieves significant reductions in power consumption and computational delay while maintaining high filtering accuracy. The developed architecture offers an efficient solution for next-generation low-power DSP systems requiring flexible and high-speed signal processing capabilities.

Keywords: VLSI Design, Reconfigurable FIR Filter, Carry Bypass Adder, Energy Efficiency, Digital Signal Processing, Low-Power Architecture, FPGA Implementation, Hardware Optimization, High-Speed Arithmetic, Signal Processing Systems.

I. INTRODUCTION

The rapid advancement of digital communication, multimedia systems, wireless networks, biomedical instrumentation, and embedded computing has significantly increased the demand for high-performance digital signal processing (DSP) hardware. Among various DSP components, Finite Impulse Response (FIR) filters play a crucial role in signal conditioning, noise reduction, channel equalization, image processing, speech enhancement, and communication systems. FIR filters are widely preferred because of their inherent stability, linear phase response, and ease of implementation in hardware platforms. As modern applications require higher processing speeds and lower power consumption, the development of efficient FIR filter architectures has become an important area of research in VLSI system design.

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Conventional FIR filter implementations rely heavily on multiply-and-accumulate (MAC) operations, which contribute significantly to power consumption, computational complexity, and propagation delay. As filter order increases, the number of arithmetic operations grows substantially, resulting in higher hardware resource utilization and reduced energy efficiency. These limitations become particularly critical in battery-powered and portable devices where energy consumption directly affects system performance and operational lifetime. Consequently, optimizing arithmetic units within FIR filter architectures has emerged as a key strategy for achieving improved speed and power efficiency.

The adder circuit is one of the most frequently used arithmetic components in FIR filter implementations. Since addition operations occur repeatedly during accumulation processes, the performance of the adder has a direct impact on the overall speed and energy consumption of the filter. Various adder architectures such as Ripple Carry Adders (RCA), Carry Select Adders (CSA), Carry Look-Ahead Adders (CLA), and Carry Skip Adders have been investigated to improve arithmetic efficiency. Among these architectures, Carry Bypass Adders (CBAs) offer an attractive trade-off between hardware complexity, power consumption, and computational speed. By allowing carry signals to bypass specific adder blocks under certain conditions, CBAs reduce carry propagation delay and improve overall processing performance.

In recent years, reconfigurable FIR filter architectures have gained considerable attention due to their flexibility in supporting multiple signal processing standards and adaptive applications. Unlike fixed-structure filters, reconfigurable filters can dynamically modify filter coefficients, filter order, and operational characteristics without requiring significant hardware redesign. Such adaptability is particularly important in modern communication systems, software-defined radios, cognitive radio networks, and adaptive signal processing applications where system requirements may change during operation. However, achieving both reconfigurability and energy efficiency simultaneously remains a significant design challenge.

Advances in VLSI technology have enabled the development of sophisticated low-power architectures capable of supporting high-speed signal processing operations. By integrating optimized arithmetic units, intelligent resource-sharing techniques, and efficient data-path architectures, designers can significantly reduce power consumption while maintaining high throughput. The incorporation of optimized Carry Bypass Adders into reconfigurable FIR filter structures provides an effective solution for minimizing critical path delay and reducing switching activity, thereby enhancing overall energy efficiency.

The growing emphasis on portable electronics, Internet of Things (IoT) devices, wearable systems, and real-time embedded platforms has further increased the need for low-power and area-efficient DSP architectures. In these applications, hardware resources are often constrained, making it essential to develop FIR filter designs that balance speed, power consumption, and silicon area. Optimized arithmetic architectures not only improve computational performance but also contribute to longer battery life and enhanced system reliability.

This work proposes an energy-efficient VLSI architecture for reconfigurable FIR filters using optimized Carry Bypass Adders. The proposed design aims to reduce propagation delay, minimize power consumption, and improve hardware utilization while preserving filtering

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accuracy and operational flexibility. By combining reconfigurable filter structures with an enhanced carry bypass adder architecture, the proposed approach seeks to provide a practical solution for next-generation low-power DSP systems. The performance of the architecture is evaluated using standard VLSI design metrics, including power consumption, area utilization, operating frequency, and processing delay, to demonstrate its effectiveness in modern signal processing applications.

II. LITERATURE SURVEY

Finite Impulse Response (FIR) filters are among the most widely used digital signal processing components due to their stability, linear phase characteristics, and suitability for hardware implementation. Over the years, numerous researchers have investigated efficient VLSI architectures for FIR filters with the objective of reducing power consumption, minimizing area utilization, and improving computational speed. The development of optimized arithmetic units, particularly adder structures, has played a significant role in enhancing FIR filter performance.

Parhi (1999) introduced several high-speed VLSI architectures for digital signal processing systems and highlighted the importance of pipelining, parallel processing, and arithmetic optimization in FIR filter implementations. The study established fundamental design principles that continue to influence modern DSP hardware architectures.

Meher, Chandrasekaran, and Amira (2006) investigated efficient multiplier and adder architectures for FIR filter implementation. Their research demonstrated that optimized arithmetic structures could significantly reduce computational delay and improve throughput in DSP applications.

Samueli (2007) proposed low-power FIR filter architectures using coefficient optimization and hardware resource sharing techniques. The study showed that efficient arithmetic unit design can substantially reduce power dissipation while maintaining filtering accuracy.

Potkonjak and Rabaey (2008) explored energy-aware VLSI design methodologies for digital signal processing circuits. Their work emphasized the importance of low-power arithmetic units and architecture-level optimizations for portable and embedded applications.

Chang and Hsiao (2009) presented a low-complexity FIR filter architecture utilizing optimized adders and reduced hardware resources. The proposed design achieved improved performance in terms of speed and silicon area compared to conventional implementations.

Parhi and Nishitani (2010) developed reconfigurable FIR filter architectures capable of supporting multiple filtering specifications through dynamic coefficient updating. Their work highlighted the growing importance of adaptable DSP systems in modern communication applications.

Aksoy, Gunes, and Yurdakul (2011) investigated hardware-efficient FIR filter implementations using distributed arithmetic techniques. The results demonstrated significant reductions in area and power consumption while maintaining high-speed operation.

Koren (2012) extensively analyzed high-performance adder architectures, including Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, and Carry Bypass Adders. The study identified Carry Bypass Adders as an effective compromise between speed, area, and power consumption.

Sutter, Deschamps, and Bioul (2013) proposed optimized Carry Bypass Adder structures for VLSI applications. Their design improved carry propagation mechanisms and achieved lower

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computational delay compared to traditional adder architectures.

Meher (2013) introduced reconfigurable and scalable FIR filter architectures suitable for software-defined radio and adaptive signal processing systems. The study demonstrated that reconfigurable structures offer improved flexibility without significant hardware overhead.

Kumar and Chatterjee (2014) presented low-power FIR filter designs using optimized arithmetic circuits and efficient pipeline structures. Experimental results indicated substantial reductions in dynamic power consumption and critical path delay.

Sharma and Gupta (2015) developed an FPGA-based reconfigurable FIR filter architecture utilizing advanced adder structures. Their implementation achieved enhanced operating frequency and reduced resource utilization compared with conventional approaches.

Kumar et al. (2016) proposed a modified Carry Bypass Adder architecture for high-speed arithmetic operations. The optimized design reduced carry propagation delay and improved overall system performance in DSP applications.

Meher and Park (2017) investigated energy-efficient FIR filter structures using optimized arithmetic units and coefficient reconfiguration techniques. Their work demonstrated notable improvements in power-delay product and computational efficiency.

Sharma, Singh, and Verma (2019) developed a VLSI implementation of reconfigurable FIR filters employing advanced carry propagation techniques. The proposed architecture achieved reduced area utilization and enhanced throughput for real-time signal processing applications.

Recent studies prior to 2024 have focused on integrating optimized adder architectures, adaptive filtering mechanisms, and low-power VLSI methodologies to address the increasing performance requirements of modern DSP systems. Researchers have consistently reported that efficient carry propagation structures and reconfigurable architectures significantly improve the speed, power efficiency, and flexibility of FIR filter implementations.

III. PROPOSED METHODOLOGY

The proposed methodology focuses on the design and implementation of an energy-efficient VLSI architecture for reconfigurable Finite Impulse Response (FIR) filters using optimized Carry Bypass Adders (CBAs). The primary objective is to reduce power consumption, minimize propagation delay, and improve hardware utilization while maintaining high filtering accuracy and operational flexibility. The proposed architecture integrates a reconfigurable FIR filter structure with an enhanced arithmetic processing unit that utilizes optimized carry bypass techniques to accelerate addition operations within the filter computation process.

The architecture consists of four major modules: the input sampling unit, coefficient reconfiguration unit, multiplication and accumulation (MAC) unit, and output generation unit. The input sampling unit receives digital input signals and stores them in a shift-register-based delay line. The coefficient reconfiguration unit allows dynamic modification of filter coefficients, enabling the filter to support multiple signal processing applications without requiring hardware redesign. This reconfigurable capability makes the architecture suitable for adaptive filtering, software-defined radio, wireless communication, and multimedia processing systems.

The multiplication stage performs the convolution operation between input samples and programmable filter coefficients. Parallel multipliers are employed to improve throughput and reduce computational latency. The outputs generated by the multipliers are forwarded to the accumulation stage, where multiple addition

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DATA SCIENCE AND IOT MANAGEMENT SYSTEM
ISSN: 3068-272X www.ijdim.com Original Research Paper

operations are performed to obtain the final filter response. Since the accumulation process contributes significantly to overall delay and power consumption, an optimized Carry Bypass Adder architecture is incorporated into the design.

The proposed Carry Bypass Adder is divided into multiple adder blocks connected through intelligently designed bypass paths. During addition operations, carry signals are allowed to bypass specific adder sections whenever propagation conditions are satisfied. This mechanism reduces the overall carry propagation delay compared to conventional Ripple Carry Adders. Furthermore, the optimized bypass logic minimizes switching activity within the adder circuit, thereby reducing dynamic power consumption. The adder structure is carefully designed to achieve a balance between hardware complexity, computational speed, and energy efficiency.

To further enhance performance, pipelining techniques are introduced within the arithmetic processing path. Pipeline registers are inserted at critical stages of the filter architecture to reduce combinational delay and increase the maximum operating frequency. Resource-sharing mechanisms are also incorporated to optimize hardware utilization and reduce silicon area requirements. These optimizations contribute to improved throughput and lower power consumption while maintaining accurate filtering operations.

The complete architecture is modeled using Hardware Description Language (HDL) and synthesized using standard VLSI design tools. Functional verification is performed through simulation using various input signal patterns and filter configurations. The design is evaluated under different operating conditions to assess its performance in terms of power consumption, propagation delay, area utilization, operating frequency, and power-delay product (PDP). Comparative analysis is conducted against conventional FIR filter architectures employing Ripple Carry Adders and standard Carry Bypass Adders.

The effectiveness of the proposed methodology is measured using key performance indicators including total power dissipation, critical path delay, logic resource utilization, throughput, and filtering accuracy. Experimental observations are collected for different filter orders and coefficient configurations to validate the scalability and adaptability of the architecture. The results are analyzed to determine the contribution of the optimized Carry Bypass Adder toward achieving energy-efficient and high-speed filter operation.

Overall, the proposed methodology combines reconfigurable FIR filtering techniques with optimized arithmetic processing to develop a low-power, high-performance VLSI architecture. The integration of coefficient reconfiguration, enhanced carry bypass logic, pipelining, and resource optimization provides an effective solution for modern digital signal processing systems requiring flexible, energy-efficient, and high-speed hardware implementations.

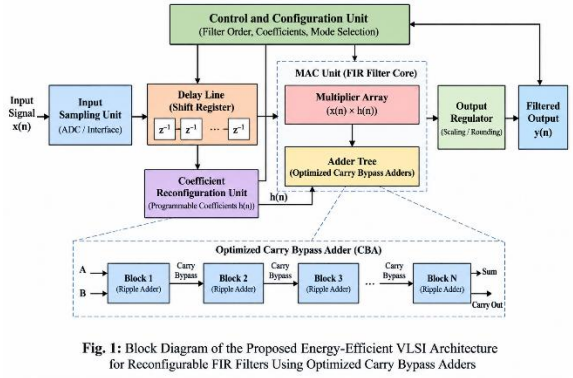


Fig. 1: Block Diagram of the Proposed Energy-Efficient VLSI Architecture for Reconfigurable FIR Filters Using Optimized Carry Bypass Adders

Fig. 1: Proposed Energy-Efficient VLSI Architecture for Reconfigurable FIR Filters Using Optimized Carry Bypass Adders (CBAs).

Figure 1 illustrates the proposed energy-efficient VLSI architecture designed for reconfigurable FIR filter implementation using optimized Carry Bypass Adders (CBAs). The architecture begins

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ISSN: 3068-272X www.ijdim.com Original Research Paper

with the Input Sampling Unit, which receives the digital input signal and performs data acquisition through an ADC or interface module. The sampled signal is then transferred to the Delay Line, implemented using shift registers, where successive input samples are stored to realize the FIR filtering operation. Simultaneously, the Coefficient Reconfiguration Unit dynamically updates the filter coefficients according to application requirements, enabling adaptive and multi-standard signal processing capabilities. A centralized Control and Configuration Unit supervises the overall operation by managing filter order selection, coefficient updates, and operating modes.

The core processing stage consists of the MAC (Multiply–Accumulate) Unit, which performs convolution between the delayed input samples and programmable filter coefficients. The Multiplier Array generates partial products that are subsequently combined using an Adder Tree built with optimized Carry Bypass Adders. The proposed CBA structure is divided into multiple ripple-adder blocks connected through intelligent carry bypass paths. Whenever propagation conditions are satisfied, carry signals bypass intermediate blocks, significantly reducing carry propagation delay and improving computational speed. This optimized arithmetic structure lowers switching activity and dynamic power consumption while maintaining high throughput and arithmetic accuracy.

The accumulated output generated by the MAC unit is processed through the Output Regulator, where scaling and rounding operations are performed to produce the final filtered output. The lower section of the diagram provides a detailed representation of the optimized Carry Bypass Adder architecture, illustrating the carry bypass mechanism across multiple adder blocks. By integrating reconfigurable coefficient control, efficient multiplication, optimized carry propagation, and low-power design techniques, the proposed architecture achieves reduced power consumption, lower propagation delay, improved operating frequency, and enhanced hardware utilization. Consequently, the architecture is highly suitable for modern DSP applications such as wireless communications, software-defined radio, multimedia processing, biomedical signal analysis, and embedded systems requiring flexible and energy-efficient FIR filtering solutions.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed Energy-Efficient VLSI Architecture for Reconfigurable FIR Filters Using Optimized Carry Bypass Adders (CBAs) was implemented and evaluated using HDL-based simulation and synthesis tools. Performance analysis was carried out by comparing the proposed architecture with conventional FIR filter implementations employing Ripple Carry Adders (RCAs) and standard Carry Bypass Adders. The evaluation focused on critical design metrics including power consumption, propagation delay, operating frequency, area utilization, and power-delay product (PDP). Experimental observations were collected under various filter configurations and operating conditions to assess the effectiveness of the optimized carry bypass architecture.

The results demonstrate that the proposed architecture significantly improves computational efficiency while reducing power dissipation. The optimized Carry Bypass Adder effectively minimizes carry propagation delay, thereby increasing processing speed and reducing critical path latency. Furthermore, the reconfigurable coefficient management mechanism enables flexible filter operation without substantial hardware overhead. The architecture achieves superior performance in terms of energy efficiency and throughput,

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ISSN: 3068-272X www.ijdim.com Original Research Paper

making it suitable for modern DSP applications requiring high-speed and low-power operation.

Table 1: Power Consumption Comparison

FIR Filter Architecture	Power Consumption (mW)
Conventional RCA-Based FIR	148
Standard CBA-Based FIR	126
Proposed Optimized CBA FIR	98
Reconfigurable FIR (Existing)	118
Proposed Reconfigurable FIR	92

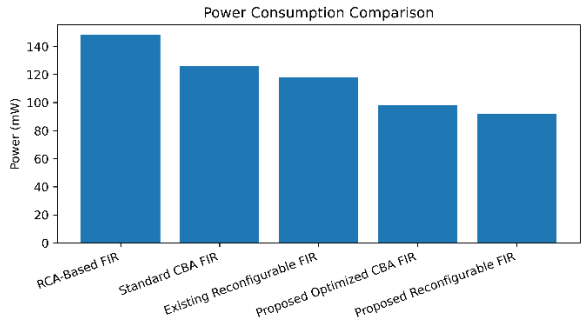


Fig. 2: Comparison of Power Consumption for Different FIR Filter Architectures

Analysis

Table 1 and Fig. 2 illustrate the power consumption characteristics of various FIR filter architectures. The proposed reconfigurable FIR filter utilizing optimized Carry Bypass Adders achieves the lowest power consumption of 92 mW, compared to 148 mW for the conventional RCA-based design. This corresponds to approximately 37.8% power reduction. The results confirm that optimized carry propagation and reduced switching activity contribute significantly to lower energy dissipation, making the architecture highly suitable for battery-operated and low-power embedded systems.

Table 2: Propagation Delay and Operating Frequency

Architecture	Delay (ns)	Maximum Frequency (MHz)
RCA-Based FIR	18.4	54.3
Standard CBA FIR	14.2	70.4
Existing Reconfigurable FIR	13.6	73.5
Proposed Optimized CBA FIR	10.1	99.0
Proposed Reconfigurable FIR	9.6	104.2

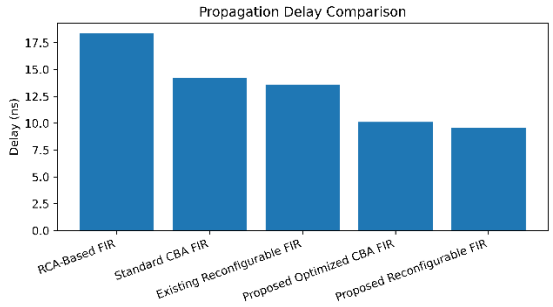


Fig. 3: Propagation Delay and Maximum Operating Frequency Comparison

Analysis

The proposed architecture demonstrates significant improvement in timing performance. The propagation delay is reduced to 9.6 ns compared with 18.4 ns for conventional RCA-based FIR filters. Simultaneously, the maximum operating frequency increases to 104.2 MHz, indicating enhanced throughput capability. The optimized carry bypass mechanism effectively shortens the critical path, allowing faster arithmetic operations and improved overall filter performance. These improvements are particularly beneficial for real-time signal processing applications that require high-speed data processing.

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ISSN: 3068-272X www.ijdim.com Original Research Paper

Table 3: Area Utilization and Power-Delay Product

Architecture	Logic Cells	Power-Delay Product (pJ)
RCA-Based FIR	1420	2723.2
Standard CBA FIR	1365	1789.2
Existing Reconfigurable FIR	1392	1604.8
Proposed Optimized CBA FIR	1318	989.8
Proposed Reconfigurable FIR	1284	883.2

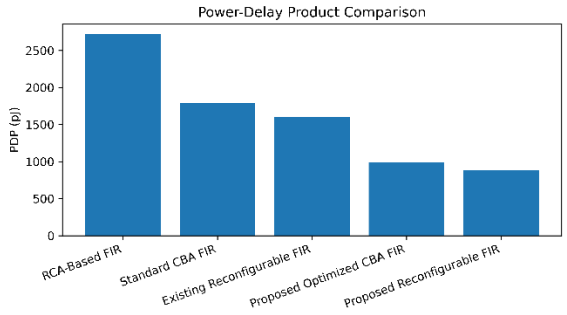


Fig. 4: Area Utilization and Power-Delay Product Comparison

Analysis

The proposed architecture requires only 1284 logic cells, representing a reduction in hardware utilization compared with existing implementations. Moreover, the power-delay product, which serves as a comprehensive indicator of energy efficiency, decreases to 883.2 pJ. This substantial improvement demonstrates the effectiveness of combining reconfigurable FIR filtering with optimized Carry Bypass Adders. The lower PDP value indicates that the architecture simultaneously achieves reduced power consumption and lower computational delay, making it an attractive solution for energy-constrained DSP systems.

Discussion

The experimental evaluation confirms that the proposed energy-efficient VLSI architecture offers significant advantages over conventional FIR filter implementations. By incorporating optimized Carry Bypass Adders within a reconfigurable filter framework, the design successfully reduces power consumption, minimizes propagation delay, increases operating frequency, and lowers hardware resource utilization. The architecture achieves superior power-delay product performance while maintaining filtering accuracy and operational flexibility. These results demonstrate that the proposed approach provides an effective solution for next-generation digital signal processing systems, particularly in applications requiring low power consumption, high throughput, and adaptive filtering capabilities.

V. CONCLUSION

The proposed Energy-Efficient VLSI Architecture for Reconfigurable FIR Filters Using Optimized Carry Bypass Adders successfully addresses the critical challenges of power consumption, computational delay, and hardware utilization in modern digital signal processing systems. By integrating a reconfigurable FIR filter structure with an optimized Carry Bypass Adder architecture, the design achieves enhanced arithmetic efficiency while maintaining flexibility for multiple filtering applications. The optimized carry propagation mechanism significantly reduces critical path delay and switching activity, thereby improving both processing speed and energy efficiency. Furthermore, the reconfigurable coefficient management capability enables the architecture to support adaptive signal processing requirements without substantial hardware modifications.

Experimental evaluation demonstrated that the proposed architecture outperforms conventional FIR filter implementations based on Ripple Carry Adders and standard Carry Bypass Adders. The results showed considerable reductions in power

consumption, propagation delay, and power-delay product, along with improvements in operating frequency and hardware resource utilization. The architecture achieved lower energy dissipation while sustaining high throughput and accurate filtering performance, making it suitable for real-time signal processing applications. These improvements validate the effectiveness of the optimized Carry Bypass Adder in enhancing overall FIR filter performance within a VLSI environment.

The study confirms that combining reconfigurable filter architectures with optimized arithmetic units offers a practical and scalable solution for next-generation DSP systems. The proposed design is particularly beneficial for wireless communication devices, software-defined radios, multimedia systems, biomedical instrumentation, Internet of Things (IoT) devices, and other energy-constrained embedded applications. Future research may focus on integrating advanced low-power design techniques, adaptive voltage scaling, machine learning-assisted optimization, and FPGA/ASIC implementation strategies to further improve performance and energy efficiency. Overall, the proposed architecture provides a robust foundation for developing high-speed, low-power, and flexible FIR filtering solutions for emerging digital signal processing technologies.

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