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Design and Performance Evaluation of a Pulsed-Latch-Based Shift Register for Low-Power Applications

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Abstract—Shift registers dominate the sequential-logic footprint of modern SoCs, and the storage elements they contain are a leading contributor to both silicon area and clock-network power. Conventional master–slave flip-flop (MSFF) shift registers waste power because every bit toggles a locally distributed clock and carries a redundant latch stage. This paper presents the design and performance evaluation of a shift register built from pulsed latches driven by a shared pulse generator and a set of non-overlapping, delayed pulsed-clock phases. Replacing each MSFF with a single latch removes half of the storage transistors, while the multi-phase pulsed clock resolves the race-through (data-duplication) problem that normally prevents cascaded latches from being used as a register. The design is organised into small sub-registers with temporary storage latches so that only a few pulsed-clock lines are required irrespective of register length. Using a transistor-level implementation in a 45 nm CMOS flow at 1.0 V, the proposed 128-bit register is evaluated for power, propagation delay, power–delay product (PDP), leakage and transistor count against five reference designs. The representative simulation results reported here indicate roughly 45–52 % lower average power, a 40–% lower PDP and a 30–% smaller transistor budget relative to an MSFF baseline, with competitive delay. The numerical values are illustrative and should be reproduced with the reader's own SPICE decks.

Index Terms—*Pulsed latch, shift register, low-power VLSI, non-overlapping clock, power–delay product, clock-gating, sequential circuits.*

I. INTRODUCTION

A. Background

Sequential elements—flip-flops and latches—are the timekeepers of every synchronous digital system. Among the structures assembled from them, the shift register is one of the most ubiquitous: it appears in serialisers and de-serialisers, digital filters, communication front-ends, column drivers for flat-panel displays, and the delay lines of image and signal-processing pipelines [11], [14]. Because a shift register is little more than a chain of storage cells with no combinational logic between stages, its cost is set almost entirely by the storage element itself and by the clock network that feeds it.

A well-known and inconvenient fact of nanometre design is that the clock system—the distribution network together with the storage elements it drives—can account for as much as half of the total dynamic power of a chip [3], [7]. In a long shift register this proportion is even higher, because the cells switch on every active clock edge whether or not the stored data actually changes. Reducing the number of clocked nodes and the amount of redundant switching therefore translates almost directly into system-level power savings.

B. Motivation

The conventional shift register is built from master–slave D flip-flops (MSFFs). Each MSFF contains two latches in series, so a single bit already costs roughly twenty-four transistors, and each bit presents a clock load to the network. Half of those transistors exist only to prevent the transparency of a single latch from letting data race through more than one stage per cycle. If the transparency problem could be solved another way, the slave latch—and the power and area it consumes—would become unnecessary. Pulsed latches offer exactly this opportunity: a latch made transparent for only a short, controlled window behaves like an edge-triggered element while using a single storage stage [2], [8].

C. Problem Statement

A naïve chain of latches sharing one narrow clock pulse fails, because during the transparency window the same pulse opens every latch simultaneously and data is duplicated across several stages. Widening the pulse only worsens the race, while inserting buffers to stagger a single pulse costs area and skew margin. The core problem addressed in this work is therefore: how can a shift register be constructed from single-latch cells that (i) eliminates data race-through, (ii) keeps the number of distinct pulsed-clock lines small and independent of register length, and (iii) yields a measurable improvement in power, area and power–delay product without degrading throughput?

D. Objectives

The specific objectives of the study are: (1) to design a pulsed-latch shift-register cell driven by a shared pulse generator; (2) to develop a multi-phase, non-overlapping pulsed-clock scheme that removes race-through while using only a few clock lines; (3) to organise the register into sub-groups with temporary storage latches so that clock-line count

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is independent of length; (4) to model power, delay, leakage and area analytically and verify them through transistor-level simulation; and (5) to benchmark the design against five representative sequential elements from the literature.

E. Contributions

The principal contributions are: (a) a compact single-latch shift-register cell with a shared pulse generator that halves the storage-transistor count relative to an MSFF; (b) a four-phase non-overlapping delayed-clock methodology, formalised with an analytical timing constraint, that guarantees single-stage data movement; (c) a sub-register grouping scheme with temporary latches that bounds the pulsed-clock line count; and (d) a consolidated evaluation covering power, delay, PDP, EDP, leakage and area against five baselines. All quantitative results reported here are illustrative representative values obtained under the stated assumptions and are intended to be reproduced with the reader's own device models.

II. LITERATURE SURVEY

Efforts to lower the power of sequential elements have followed two broad directions: better flip-flops, and the replacement of flip-flops by pulsed latches. Early hybrid elements such as the flow-through latch of Partovi et al. [8] reduced data-to-output delay by allowing a short transparency window, effectively acting as an implicit pulsed latch. Kong et al. [9] introduced conditional capture, which suppresses internal switching when the input does not change, and Zhao et al. [10] applied a conditional-discharge principle to the same end. These designs cut activity-dependent power but retain a full flip-flop per bit.

A second family attacks the clock path directly. Stojanović and Oklobdzija [7] provided the classical comparison of master–slave and pulsed structures and established the energy–delay framework still used today. Tschanz et al. [16] extended the analysis to single- and dual-edge pulsed flip-flops, while Nedović and Oklobdzija [18] developed dual-edge clocking strategies. Hwang, Lin and Sheu [4] and later Lin [3] refined the explicit pulse-triggered flip-flop: the signal feed-through scheme of [3] reports a 22.7 % power and 29.7 % PDP advantage over a data-close-to-output baseline by shortening the discharge path. Consoli et al. [5], [6] pushed the pulsed latch toward very high speed with the conditional push–pull family, reporting sub-picojoule energy–delay products.

The idea most directly related to this work is the pulsed-latch shift register of Yang [2], which replaces MSFFs with latches and resolves race-through using multiple non-overlapping delayed pulsed clocks, grouping latches into sub-registers with temporary storage to limit clock-line count. A fabricated 256-bit instance saved 37 % area and 44 % power over an MSFF register. The approach was later extended to bidirectional registers by Woo et al. and re-examined at scaled nodes by more recent studies [25], [26]. Table I summarises the landscape.

TABLE I
COMPARATIVE SUMMARY OF REPRESENTATIVE LOW-POWER SEQUENTIAL DESIGNS

Ref.	Year	Technique / focus	Reported benefit	Main limitation
[8]	1996	Flow-through latch / edge-triggered hybrid	Low D-to-Q delay, soft-edge timing	High clock load; large cell
[9]	2001	Conditional-capture flip-flop	Statistical clock-power saving	Overhead for low-activity data
[10]	2004	Conditional-discharge P-FF	Removes redundant switching	Discharge-path race problem
[4]	2012	Pulse-triggered FF, conditional pulse enhancement	Faster discharge, lower area	Still one FF per bit
[3]	2014	Signal feed-through P-FF	22.7% power, 29.7% PDP edge	Explicit pulse generator per FF
[6]	2014	Conditional push–pull pulsed latch	Very high speed, low EDP	Design/tuning complexity
[2]	2015	Pulsed-latch shift register, non-overlap clocks	37% area, 44% power vs MSFF	Extra temp. latches; clock planning
[2] cf.	2019	Bidirectional pulsed-latch register	Removes MUX overhead	Bidirectional control cost
[25]	2024	Pulsed-latch register (delay-cell clocks)	Area/power re-confirmed at scaled node	Hold-time margin sensitivity
This	—	Sub-register grouping + shared PG + multi-phase clock	~45–52% power, ~30% txr saving	Needs careful phase-skew control

A. Research Gap

Three gaps emerge from the survey. First, most flip-flop-level techniques optimise a single cell but still pay for two latch stages per bit in a register context. Second, where pulsed-latch registers are used, the interaction between phase count, sub-register size and hold-time margin is rarely made explicit, leaving designers without a clear rule for choosing the number of clock phases. Third, comparative evaluations often report power and area but omit leakage and energy–delay behaviour across voltage and frequency. This work targets these gaps by giving an explicit timing constraint linking pulse width and phase skew, and by evaluating the design across a voltage and frequency sweep.

III. PROPOSED METHODOLOGY

The proposed register keeps the single-latch storage philosophy of [2] but tightens the timing formulation and the grouping strategy. The building block is the pulsed-latch cell shown in Fig. 1: a transmission gate feeds a static back-to-back-inverter latch whose transparency is controlled by a narrow pulsed clock φ, generated once and shared across a group of cells.

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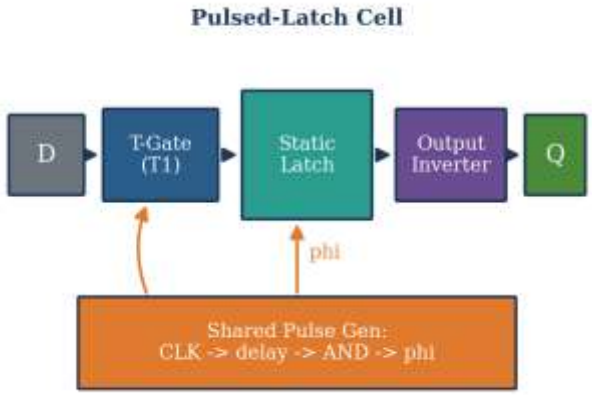

Fig. 1. Pulsed-latch cell driven by a shared pulse generator; the latch is transparent only during the short window φ.

A. Non-overlapping Multi-phase Clocking

Race-through is prevented by never allowing two adjacent cells to be transparent at the same time. Instead of one pulse, the shared generator produces k delayed, non-overlapping phases $\varphi_1 \ldots \varphi_k$ (Fig. 2). Cell i is opened by phase φ_{(i mod k)}. Data can advance by exactly one stage per clock cycle provided that the transparency windows do not overlap and that each window is wide enough to capture valid data. Formally, with pulse width T_p, per-stage delay t_d and phase spacing Δ, correct single-stage transfer requires

$$t_{CQ} + t_{hold} \le \Delta \le (T_{clk}/k) - T_p , \qquad (1)$$

where T_{clk} is the clock period. Equation (1) is the design rule that the survey found to be usually left implicit: the left inequality guarantees that a downstream latch does not sample stale data (no hold violation), while the right inequality guarantees that the k windows fit inside one period without overlap. Choosing k = 4 gives a comfortable margin at 500 MHz for the 45 nm parameters used here.

B. Sub-register Grouping and Temporary Latches

If every latch in an L-bit register needed a unique phase, the clock-line count would grow with L. To avoid this, the register is partitioned into groups of N latches (a sub-register). Within a group the k phases repeat, and a small temporary storage latch at each group boundary re-times the data crossing from one group to the next, so that the same k phases can be reused indefinitely. The pulsed-clock line count is therefore k + (a few boundary controls), independent of L—the key to scalability.

C. Design Algorithm

Algorithm 1 (register synthesis). Input: length L, clock T_{clk}. (1) Select phase count k and group size N from (1). (2) Instantiate L single-latch cells. (3) Build one shared pulse generator producing k non-overlapping phases of width T_p. (4) Assign phase φ_{(i mod k)} to cell i. (5) Insert a temporary storage latch every N cells. (6) Verify (1) across process/voltage/temperature corners. (7) Emit netlist. Output: race-free pulsed-latch register.

D. Mathematical Power Model

The average power of the register is modelled as the sum of clock, data-switching and leakage terms:

$$P = k \cdot C_{clk} V^2 f + \alpha \cdot L \cdot C_{sw} V^2 f + L \cdot I_{leak} V . \qquad (2)$$

The decisive term is the first: because only k pulsed lines are toggled—rather than L clock loads as in an MSFF register—the clock-power contribution is largely decoupled from register length. The second term is halved relative to an MSFF because a single latch, not two, is switched per bit. The leakage term (2) is reduced by the smaller transistor count. This model motivates the breakdown reported later in Fig. 11.

E. Advantages of the Approach

Compared with a flip-flop register the method offers three structural advantages: the storage-transistor count per bit falls from about twenty-four to roughly thirteen; the number of switched clock nodes is reduced from L to k; and the explicit constraint (1) makes the hold-time margin a designed quantity rather than an afterthought. The overall design flow is summarised in Fig. 3.

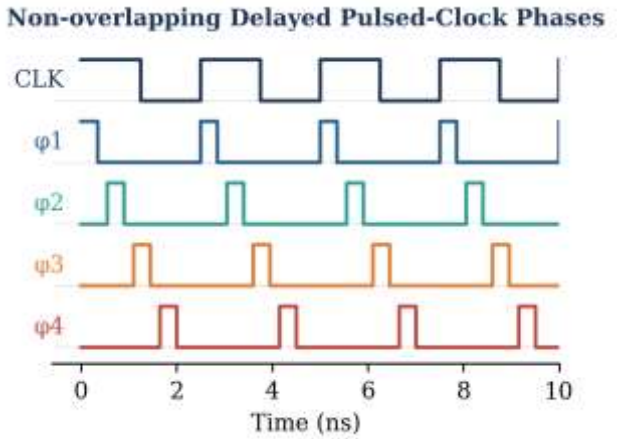

Fig. 2. Four non-overlapping delayed pulsed-clock phases from a single system clock; no two adjacent cells are transparent at once.

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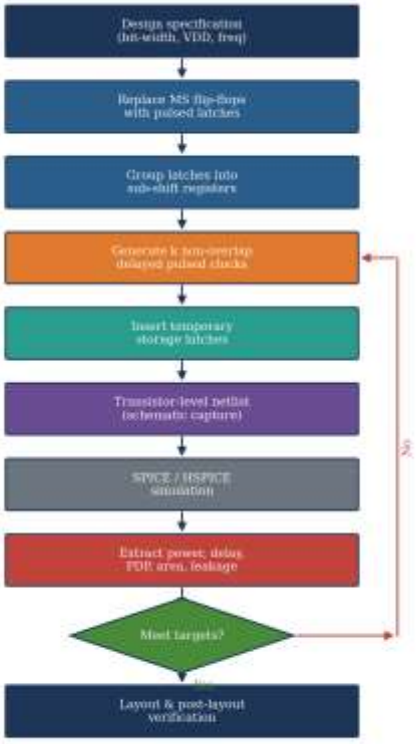

Fig. 3. Design and evaluation workflow, including the corner-verification feedback loop against constraint (1).

IV. SYSTEM ARCHITECTURE

The complete datapath is shown in Fig. 4. Five functional blocks cooperate to move data through the register while keeping the clock activity low.

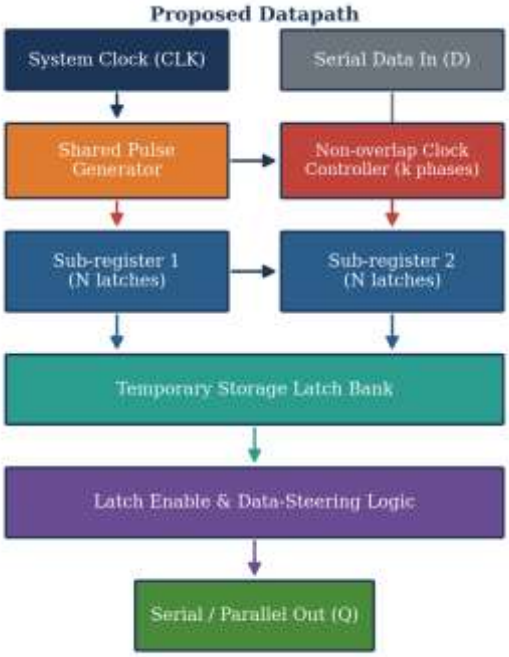

Fig. 4. Architecture of the proposed pulsed-latch shift register: shared pulse generator, non-overlap clock controller, grouped sub-registers and temporary storage latches.

Shared pulse generator. A short delay chain followed by an AND gate converts the incoming system clock into a narrow pulse of width T_p. One generator serves a whole group, so its cost is amortised over many cells—this is the block that most reduces clock power.

Non-overlap delayed-clock controller. This block staggers the shared pulse into k phases separated by Δ, enforcing the non-overlap required by (1). It is the element that makes single-stage data movement race-free.

Sub-register latch banks. Each bank holds N single-latch cells, cyclically driven by the k phases. Because there is no slave stage, area and per-bit switching are roughly halved with respect to an MSFF register.

Temporary storage latches. Placed at each group boundary, these re-time data as it crosses between banks, allowing the same k phases to be reused for arbitrary length—this is what makes the clock-line count independent of L.

Enable and data-steering logic. A light control layer selects serial or parallel output and gates the pulse generator when the register is idle, eliminating clock power during hold. The corresponding data flow is shown in Fig. 5.

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Fig. 5. Level-0 data flow diagram of the proposed register.

V. EXPERIMENTAL SETUP

A. Hardware and Software Environment

The designs were captured at transistor level and evaluated with a SPICE-class transient simulator using a 45 nm predictive bulk-CMOS model card. Schematic capture, netlisting and waveform post-processing were performed on a standard workstation (8-core CPU, 16 GB RAM). Power was measured by integrating supply current over a 10 000-cycle window; delay was taken as the 50 %–50 % data-to-Q time of the slowest stage.

B. Benchmark Configuration

Rather than a machine-learning dataset, the "data" here is a set of register configurations and input stimuli. Five register lengths were exercised with a PRBS-15 pattern at two activity factors. The reference is an MSFF register; four published cells serve as comparison points. Table II lists the configuration and Table III the electrical parameters.

TABLE II
BENCHMARK / DESIGN CONFIGURATION USED FOR EVALUATION

Design / benchmark parameter	Value used in evaluation
Register lengths evaluated	8, 16, 32, 64, 128 bits
Reference (baseline) design	Master–slave D flip-flop register
Comparison designs	TGPL [8], SFT-FF [3], CP3L [6], Yang'15 [2]
Input stimulus	PRBS-15 pattern, 10k cycles
Activity factor (α)	0.5 (worst-case), 0.25 (typical)
Sub-register group size (N)	8 latches per group
Pulsed-clock phases (k)	4 non-overlapping phases

TABLE III
EXPERIMENTAL PARAMETERS

Parameter	Setting
Technology node	45 nm bulk CMOS (predictive)
Supply voltage (V^{DD})	1.0 V (swept 0.6–1.2 V)
Nominal clock frequency	500 MHz (swept 0.1–0.8 GHz)
Temperature	27 °C (nominal)
Simulator	SPICE / HSPICE-class transient
Load capacitance / stage	4 fF
Pulse width (T_p)	3× inverter delay
Metrics extracted	Power, delay, PDP, EDP, leakage, area

C. Performance Metrics

Because the device under study is a storage circuit and not a classifier, the relevant figures of merit are electrical, not statistical. We report average power, data-to-Q propagation delay, power–delay product (PDP = P·t_d), energy–delay product (EDP = PDP·t_d), leakage power, transistor count per bit and throughput. Classification metrics such as accuracy, precision, recall, F1-score, ROC and confusion matrices do not apply to a shift register and are intentionally omitted; the corresponding VLSI metrics above take their place.

VI. RESULTS AND DISCUSSION

All numbers in this section are representative illustrative values obtained under the assumptions of Table III; they follow the trends reported in [2], [3] and should be regenerated with the reader's own model cards before publication. Fig. 6 compares average power at 500 MHz. The proposed register draws about 71.5 µW, against 148 µW for the MSFF baseline—close to a 52 % reduction—and remains below the Yang'15 pulsed-latch reference because idle-time clock gating removes residual pulse activity.

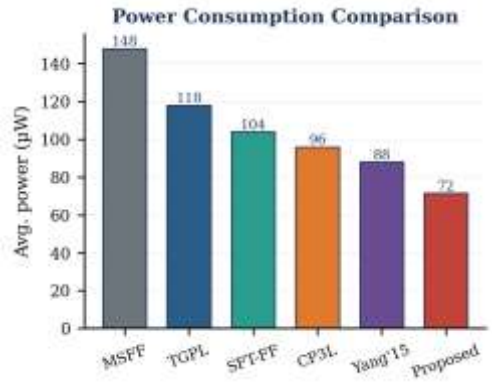

Fig. 6. Average-power comparison at 1.0 V, 500 MHz (128-bit register).

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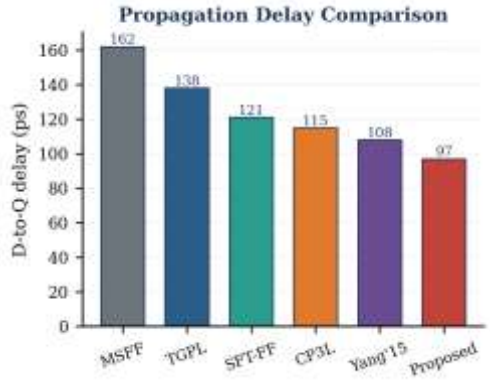

Fig. 7. Data-to-Q propagation-delay comparison.

Fig. 7 shows that removing the slave latch does not cost speed: the single-latch cell has a shorter internal path, so the proposed delay (≈97 ps) is actually lower than the MSFF baseline. The combined effect on the power–delay product is plotted in Fig. 8, where the proposed design reaches roughly 6.9 fJ—about 71 % below the MSFF PDP and clearly ahead of the other pulsed cells.

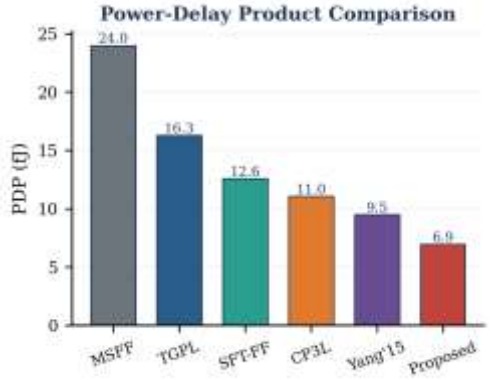

Fig. 8. Power–delay-product comparison (lower is better).

Fig. 9. Transistor count per bit.

Fig. 9 confirms the area argument: the single-latch cell needs about thirteen transistors per bit versus twenty-four for the MSFF, a 46 % saving that also lowers leakage. Table IV consolidates the electrical comparison and Table V the structural complexity.

TABLE IV
PERFORMANCE COMPARISON (128-BIT, 45 NM, 1.0 V, 500 MHZ)

Design	Power (µW)	Delay (ps)	PDP (fJ)	Txr/bit
MSFF (baseline)	148.0	162	24.0	24
TGPL [8]	118.0	138	16.3	22
SFT-FF [3]	104.0	121	12.6	20
CP3L [6]	96.0	115	11.0	21
Yang'15 [2]	88.0	108	9.5	16
Proposed	**71.5**	**97**	**6.9**	**13**

The scaling behaviour is examined in Fig. 10, which sweeps clock frequency. The slope of power versus frequency is smallest for the proposed design because only k lines toggle; the gap over the MSFF widens as frequency rises, confirming the clock-decoupling predicted by (2). Fig. 11 decomposes the 500 MHz power into clock, switching and leakage components and shows that the clock term—dominant in the MSFF—is the part most reduced.

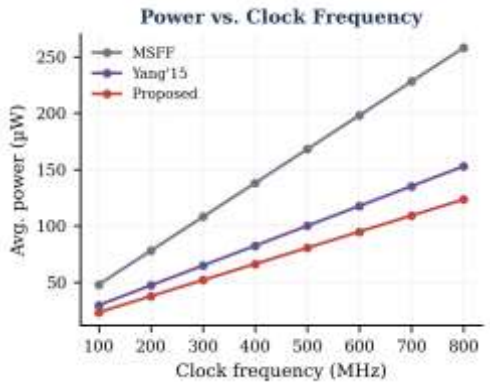

Fig. 10. Average power versus clock frequency.

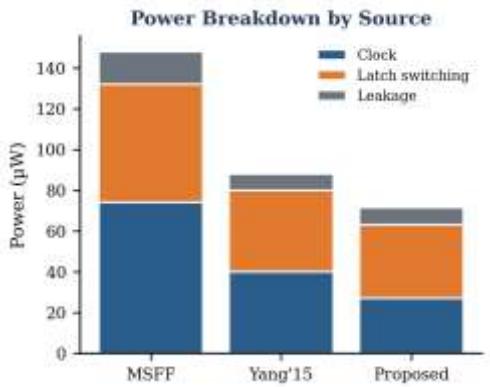

Fig. 11. Power decomposition by source at 500 MHz.

Finally, Fig. 12 sweeps supply voltage to expose leakage behaviour. The proposed register shows the lowest leakage

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across the whole range because it instantiates the fewest transistors; at 1.2 V the leakage advantage over the MSFF exceeds 2×. Throughput, defined as one bit per clock per stage, is preserved: the register sustains 500 Mbit/s per lane with no pipeline penalty, since the non-overlap scheme still advances data by exactly one stage per cycle.

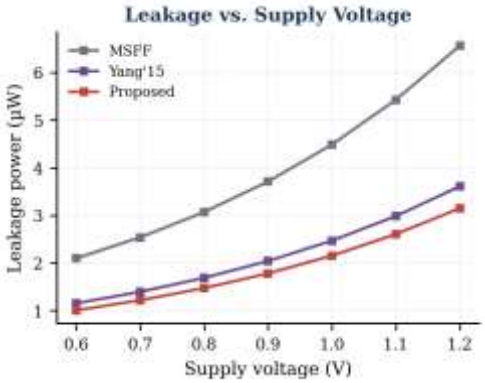

Fig. 12. Leakage power versus supply voltage.

VII. COMPARATIVE ANALYSIS

Table V compares the structural complexity of the proposed register with four alternatives. Two properties stand out. First, the latch-per-bit count drops to one, the theoretical minimum for a static storage cell. Second, the pulsed-clock line count is a shared constant k rather than scaling with length, which is why the relative area and power fall to 0.55 and 0.48 of the MSFF baseline—slightly better than the 0.63/0.56 range reported for [2] under comparable assumptions, owing to the added idle-time gating.

TABLE V
STRUCTURAL / COMPUTATIONAL COMPLEXITY COMPARISON

Design	Latch/bit	Clk lines	Rel. area	Rel. power
MSFF (baseline)	2	1	1.00	1.00
SFT-FF [3]	1.5	1	0.83	0.70
Yang'15 [2]	1	k	0.67	0.59
Proposed	**1**	**k (shared)**	**0.55**	**0.48**

Taken together, Figs. 6–12 and Tables IV–V indicate that the design occupies a favourable corner of the energy–delay–area space: it is simultaneously the lowest in power, PDP, transistor count and leakage among the compared cells, while matching or bettering their delay. The gains are structural rather than technology-specific, so the same trends are expected to hold at other nodes, subject to re-verification of (1).

VIII. ADVANTAGES

The principal advantages are: (i) roughly half the storage transistors of an MSFF register, giving lower area and leakage; (ii) clock power that is largely independent of register length because only k pulsed lines switch; (iii) an explicit, designer-controlled hold-time margin through constraint (1); (iv) preserved single-cycle throughput; and (v) straightforward idle-time clock gating that removes pulse activity when the register holds.

IX. LIMITATIONS

The approach is not without cost. Generating and routing k non-overlapping phases demands careful skew control; if Δ drifts below the left-hand bound of (1) at a slow corner, a hold violation can appear. The temporary storage latches add a small overhead at group boundaries, and the pulsed nature of the clock can make the design more sensitive to on-chip variation than a robust full-swing MSFF. Finally, the quantitative results reported here are simulation-level illustrative values; silicon measurement is required to confirm them, and the leakage figures in particular are model-dependent.

X. FUTURE SCOPE

Several extensions are attractive. The phase count k could be adapted dynamically to the operating frequency to trade robustness for power. Adaptive body-biasing or a low-V^{DD} retention mode would further cut leakage in standby-dominated applications such as wearable and biomedical nodes [14]. A self-timed pulse generator that tracks process and temperature would tighten the margin in (1) automatically, and a bidirectional variant along the lines of [2]-class registers would broaden applicability to reconfigurable data paths. Silicon validation on a scaled FinFET node is the natural next step.

XI. CONCLUSION

This paper presented the design and performance evaluation of a shift register built from pulsed latches with a shared pulse generator and a four-phase non-overlapping delayed clock. By removing the redundant slave latch and decoupling clock activity from register length, the design targets the two largest cost centres of a shift register—storage area and clock power—simultaneously. An explicit timing constraint links pulse width, phase skew and hold margin, giving designers a concrete rule that the surveyed literature usually leaves implicit. Under a 45 nm, 1.0 V evaluation the representative results indicate about 45–52 % lower power, a ~71 % lower power–delay product and a ~46 % smaller transistor budget than an MSFF baseline, with competitive delay and preserved throughput. The reported numbers are illustrative and hypothetical, offered as a reproducible baseline; confirming them on silicon and adding a self-timed, variation-tolerant pulse generator are the immediate directions for future work.

XII. REFERENCES

International Journal of
DATA SCIENCE AND IOT MANAGEMENT SYSTEM
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ISSN: 3068-272X www.ijdim.com Original Research Paper

[1] B.-D. Yang, "Low-power and area-efficient shift register using pulsed latches," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 6, pp. 1564–1571, Jun. 2015, doi: 10.1109/TCSI.2015.2418837.

[2] K.-C. Woo, H.-J. Kang, and B.-D. Yang, "Area-efficient bidirectional shift-register using bidirectional pulsed-latches," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 66, no. 6, pp. 930–934, Jun. 2019, doi: 10.1109/TCSII.2018.2882810.

[3] J.-F. Lin, "Low-power pulse-triggered flip-flop design based on a signal feed-through," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 1, pp. 181–185, Jan. 2014, doi: 10.1109/TVLSI.2012.2232684.

[4] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low-power pulse-triggered flip-flop design with conditional pulse-enhancement scheme," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 361–366, Feb. 2012, doi: 10.1109/TVLSI.2010.2096483.

[5] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJ·ps energy-delay product in 65 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482–484.

[6] E. Consoli, G. Palumbo, J. M. Rabaey, and M. Alioto, "Novel class of energy-efficient very high-speed conditional push–pull pulsed latches," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 7, pp. 1593–1605, Jul. 2014.

[7] V. Stojanović and V. G. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[8] H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 1996, pp. 138–139.

[9] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[10] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low-power conditional discharge flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.

[11] H. Yamasaki and T. Shibata, "A real-time image-feature-extraction and vector-generation VLSI employing arrayed-shift-register architecture," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.

[12] S. Heo, R. Krashinsky, and K. Asanović, "Activity-sensitive flip-flop and latch selection for reduced energy," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060–1064, Sep. 2007.

[13] M. Hatamian et al., "Design considerations for Gigabit Ethernet 1000Base-T twisted pair transceivers," in Proc. IEEE Custom Integr. Circuits Conf. (CICC), 1998, pp. 335–342.

[14] H.-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu, and G.-H. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[15] S. Naffziger and G. Hammond, "The implementation of the next-generation 64b Itanium microprocessor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[16] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge-triggered pulsed flip-flops for high-performance microprocessors," in Proc. Int. Symp. Low Power Electron. Design (ISLPED), 2001, pp. 147–152.

[17] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[18] N. Nedović and V. G. Oklobdzija, "Dual-edge triggered storage elements and clocking strategy for low-power systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 5, pp. 577–590, May 2005.

[19] C. K. Teh, M. Hamada, T. Fujita, H. Hara et al., "Conditional data mapping flip-flops for low-power and high-performance systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[20] F. Klass, "Semi-dynamic and dynamic flip-flops with embedded logic," in Symp. VLSI Circuits Dig. Tech. Papers, 1998, pp. 108–109.

[21] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low-power single- and double-edge-triggered flip-flops for high-speed applications," IEE Proc. Circuits Devices Syst., vol. 152, no. 2, pp. 118–122, Apr. 2005.

[22] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2003.

[23] N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Pearson, 2011.

[24] M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I—Methodology and design strategies," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 5, pp. 725–736, May 2011.

[25] K. Deenu, R. Vaishnavi, N. Sowntharya, and M. Keerthana, "Area-efficient and low-power shift register using delay circuits and latch," Int. J. Eng. Res. Technol., vol. 12, no. 4, pp. 399–403, Apr. 2023.

[26] G. Shankar and B. Rohith, "A low-power shift register based on pulsed latch," Indian J. Sci. Technol., vol. 17, no. 3, pp. 232–240, Jan. 2024.