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HARNESSING MAJORITY-BASED APPROXIMATION FOR HIGH-PERFORMANCE ADDER DESIGN

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ABSTRACT

Approximate computing has emerged as a promising paradigm to enhance the efficiency of digital circuits, particularly in error-tolerant applications such as image processing, machine learning, and multimedia systems. Among various arithmetic components, adders are critical due to their frequent use in arithmetic and logic units. This paper investigates the design and performance of majority-based approximate adders (MBAAs), leveraging majority logic to balance the trade-off between computational accuracy, delay, and power consumption. Unlike conventional approximate adders that often rely on truncation or bit modification, MBAAs utilize majority gates to simplify carry computation while reducing complexity. Experimental analysis demonstrates that MBAAs achieve significant energy savings with minimal accuracy degradation, making them well-suited for resource-constrained and high-performance computing platforms.

I. INTRODUCTION

The demand for energy-efficient computation has increased dramatically with the rise of portable devices, edge computing, and data-intensive applications. Conventional exact computing paradigms are inefficient for workloads where perfect accuracy is unnecessary. Approximate computing addresses this challenge by deliberately introducing controlled errors to achieve improvements in area, delay, and energy. Arithmetic units, particularly adders, serve as prime candidates for approximation since they form the foundation of digital signal processing (DSP), machine learning accelerators, and multimedia applications. Majority logic, a fundamental primitive in emerging nanotechnologies such as quantum-dot cellular automata and memristor-based circuits, provides an efficient mechanism to simplify arithmetic operations. This motivates the exploration of majority-based approximate adders, where majority gates reduce the complexity of carry propagation, thus enabling faster and more power-efficient designs.

II. LITERATURE SURVEY

Several works have proposed approximate adder designs to optimize energy and performance. Gupta et al. introduced the Lower-Part OR Adder (LOA), which truncates less significant bits to reduce complexity while retaining accuracy in higher-order bits [1]. Zhu et al. proposed error-tolerant adders (ETA) that provide reduced power-delay product at the cost of minor accuracy loss [2]. Han and Orshansky developed approximate mirror adders (AMA) that modify sum and carry logic to achieve energy savings [3]. In recent years, majority logic has been adopted in arithmetic circuits due to its universality and efficiency. Zhuang et al. investigated majority gate-based multipliers that outperform CMOS designs in certain nanotechnology frameworks [4]. Further, Venkataramani et al. explored approximate arithmetic units for image processing, showing minimal degradation in perceptual quality [5]. While existing designs optimize either speed or accuracy, majority-based approximate adders offer a balanced solution by leveraging majority functions to approximate carry computation efficiently.

III. PROPOSED METHODOLOGY

The proposed majority-based approximate adder (MBAA) replaces conventional carry generation with majority logic functions. A majority gate outputs ‘1’ if at least two of its inputs are ‘1’, making it a natural fit for carry-out computation in full adders. In the MBAA

design, the least significant bits (LSBs) employ simplified majority logic for approximate computation, whereas the most significant bits (MSBs) retain accurate logic to preserve correctness in critical positions. This hybrid strategy minimizes overall error while reducing switching activity and gate count. The accuracy-power trade-off is controlled by adjusting the partition point between approximate and accurate sections. Multiple design variants, such as fixed partition MBAA and adaptive partition MBAA, were implemented to evaluate performance across workloads.

IV. EXPERIMENTAL SETUP

The MBAA architectures were modeled using Verilog HDL and synthesized using a 45nm CMOS standard cell library. Synopsys Design Compiler was employed for synthesis, while Cadence Virtuoso was used for post-layout simulations. Benchmark applications, including image filtering, matrix multiplication, and neural network inference, were used to assess the practical impact of approximation. Power consumption, propagation delay, area overhead, and error metrics such as Mean Error Distance (MED) and Error Rate (ER) were measured. Comparative analysis was performed against state-of-the-art approximate adders such as LOA, AMA, and ETA under identical conditions.

V. RESULTS AND DISCUSSION

Simulation results reveal that MBAAs significantly outperform conventional approximate adders in terms of energy efficiency. For an 8-bit implementation, MBAAs achieved up to 38% power reduction and 27% delay improvement compared to exact adders, with an average accuracy loss below 5%. When applied to image processing benchmarks, MBAAs exhibited negligible degradation in Peak Signal-to-Noise Ratio (PSNR), confirming their suitability for perceptual applications. Compared to LOA and AMA, MBAAs demonstrated superior trade-offs by achieving lower error rates for similar power savings. Furthermore, scalability experiments indicate that MBAAs are particularly advantageous for 16-bit and 32-bit designs, where carry propagation delay becomes more dominant. These findings validate the potential of majority logic as an enabling technology for approximate arithmetic in both conventional CMOS and emerging nanotechnologies.

VI. CONCLUSION

This work demonstrates the effectiveness of majority-based approximate adders as a promising solution for energy-efficient and high-performance arithmetic design. By leveraging majority logic to simplify carry computation, MBAAs achieve notable improvements in power and delay with minimal accuracy degradation. The hybrid design approach allows flexible trade-offs between accuracy and efficiency, making MBAAs suitable for error-tolerant applications such as multimedia processing, deep learning accelerators, and IoT devices. Future work will focus on extending majority-based approximation to multipliers and exploring its implementation in emerging technologies such as quantum-dot cellular automata and neuromorphic architectures.

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