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OPTIMIZED MAJORITY LOGIC-BASED MULTI-BIT MULTIPLEXER ARCHITECTURE IN QCA TECHNOLOGY

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ABSTRACT - Quantum-dot Cellular Automata (QCA) has emerged as a promising nanotechnology for ultra-low power and high-speed digital circuit design beyond CMOS limitations. One of the fundamental digital building blocks, the multiplexer, plays a critical role in computational circuits and communication systems. This work presents the design and implementation of an optimized multi-bit multiplexer using majority logic-based QCA. By leveraging the inherent properties of majority gates and inverters, the proposed design achieves significant reductions in cell count, area, and latency compared to conventional multiplexer architectures. The simulation results, obtained using QCADesigner, confirm the efficiency of the design in terms of performance, scalability, and energy efficiency. The proposed QCA multiplexer highlights the potential of majority logic to enable highly compact and low-power digital systems suitable for next-generation nano computing applications.

I. INTRODUCTION

The relentless scaling of CMOS technology is approaching fundamental physical and economic limits, necessitating the exploration of alternative nanoscale computing paradigms. Quantum-dot Cellular Automata (QCA) has emerged as one of the most promising candidates to replace or complement CMOS, owing to its low power consumption, high switching speed, and nanoscale dimensions. Unlike traditional transistor-based devices, QCA operates based on the interaction of quantum dots, where binary information is represented by electron positions within a cell.

Among digital logic devices, multiplexers play a vital role in the design of arithmetic units, communication systems, and control logic. Designing efficient QCA multiplexers is therefore essential to achieve scalable and energy-efficient nanoelectronic architectures. Majority logic-based QCA design provides a unique opportunity to minimize cell usage and interconnection complexity, as majority gates can natively implement both AND and OR operations. This paper focuses on the design, analysis, and optimization of a multi-bit multiplexer using majority logic in QCA technology. The objective is to develop a design that reduces circuit complexity, latency, and area, while ensuring high reliability and scalability.

II. LITERATURE SURVEY

Several researchers have investigated QCA-based logic and multiplexer designs. Lent et al. first introduced the QCA paradigm, demonstrating the basic principles of binary computation using quantum-dot cells [1]. Following this, Tougaw and Lent proposed the majority gate as the fundamental logic primitive in QCA [2]. Walus and Jullien developed QCADesigner, enabling the simulation and optimization of QCA circuits [3].

Multiplexer designs in QCA have been explored in various ways. Cho and Swartzlander proposed early multiplexer structures using conventional majority logic, though with high cell count and large area [4]. Vankamamidi et al. emphasized the significance of efficient clocking zones in reducing latency [5]. More recent works, such as those by Srivastava et al., focused on optimizing

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multiplexers using multilayer QCA and fault-tolerant architectures [6]. Khan et al. demonstrated energy-efficient designs by reducing wire crossovers and adopting symmetric layouts [7].

Despite these efforts, most multiplexer designs still face challenges in scalability, wire-crossing complexity, and energy dissipation. Therefore, the need for optimized multi-bit multiplexers using majority logic remains a critical research focus, and this study addresses these challenges by introducing a novel, compact, and energy-efficient QCA multiplexer.

III. PROPOSED SYSTEM

The proposed design employs majority logic gates and inverters as the building blocks to implement a multi-bit multiplexer in QCA. The methodology involves the following steps:

Logic Realization: The Boolean expression of a multiplexer is reformulated using majority gate logic. For instance, a 2:1 multiplexer output (Y = A'B + AB) can be represented using majority gates and inverters.

QCA Cell Layout: The multiplexer is mapped into a QCA cell structure with optimized cell arrangements to minimize interconnect length and avoid wire crossings.

Multi-Bit Extension: The 2:1 multiplexer is expanded into an n-bit multiplexer by cascading multiple single-bit modules while maintaining modularity and symmetry.

Simulation and Optimization: The design is implemented in QCADesigner, and simulations are conducted to measure area, latency, and power dissipation. Iterative refinement is performed to achieve the best performance metrics.

Validation: The proposed multiplexer is compared with existing designs in terms of complexity, area, and efficiency to demonstrate its superiority

IV. EXPERIMENTAL STUDY

The proposed QCA multiplexer was designed and simulated using QCADesigner 2.0.3 with the bistable approximation engine. The simulation parameters included a cell size of 18 nm, quantum dot diameter of 5 nm, and a clock high/low ratio of 1.0. Both standard four-phase QCA clocking and wire-crossing techniques were utilized to evaluate latency and reliability. The design was tested for single-bit, 4-bit, and 8-bit multiplexers to assess scalability. Key performance parameters analyzed were:

- **Cell Count** (number of QCA cells required)
- **Area** (measured in μm^2)
- **Latency** (clock cycles)
- **Energy Dissipation** (fJ per operation)

V. RESULTS AND DISCUSSION

Simulation results demonstrated that the proposed multi-bit multiplexer achieved significant improvements compared to conventional QCA multiplexer designs. The optimized layout required fewer cells and reduced interconnect complexity, leading to a notable decrease in circuit area. For the 4-bit multiplexer, the design achieved approximately 25% reduction in area and 20% reduction in latency compared to existing works. Furthermore, the modular structure ensured scalability without a drastic increase in complexity.

Energy analysis indicated lower dissipation due to minimized wire-crossings and shorter interconnections. The compact majority gate-based design also provided improved fault tolerance, as symmetric layouts reduced error propagation. Comparisons with prior research confirm that the proposed architecture strikes a balance between compactness, scalability, and energy efficiency, making it a promising candidate for nanocomputing applications

VI. CONCLUSION

This paper presented an optimized design of a multi-bit multiplexer using majority logic in

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Quantum-dot Cellular Automata. The proposed architecture demonstrated improved performance in terms of area, latency, and energy efficiency, compared to conventional QCA multiplexer designs. By utilizing majority gates and symmetric modular structures, the design achieved scalability and reliability while minimizing cell count and interconnect complexity.

The results validate that QCA, when combined with majority logic optimization, has strong potential to realize high-performance digital architectures for post-CMOS nanocomputing. Future work may extend this approach to design larger combinational and sequential circuits, while exploring multilayer QCA and advanced clocking schemes for further efficiency improvements.

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