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A NOVEL REDUCED-COMPONENT MULTILEVEL INVERTER FOR STANDALONE SOLAR ENERGY CONVERSION USING FUZZY LOGIC CONTROLLER

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ABSTRACT

A multilevel inverter (MLI) is an advanced power conversion technology capable of generating near-sinusoidal output voltage for AC applications. Increasing the number of output voltage levels enhances the waveform quality but often results in a higher component count, greater power loss, and increased system complexity. This paper proposes a novel multilevel inverter topology with a reduced number of semiconductor switches and optimized performance using a Fuzzy Logic Controller (FLC). The proposed inverter employs ten switches and two isolated DC sources, enabling multiple output voltage levels through asymmetric source management. Specifically, a 1:3 source ratio produces a seventeen-level output, while symmetric (1:1) and binary-asymmetric (1:2) configurations yield nine and thirteen levels, respectively, without altering the hardware configuration.

The integration of the Fuzzy Logic Controller ensures intelligent control of switching angles and modulation, thereby improving voltage regulation, minimizing total harmonic distortion (THD), and enhancing dynamic response under varying load and irradiance conditions. The proposed topology exhibits lower component count level (CCL), reduced total blocking voltage (TBV), lower THD, and minimal switching losses, making it highly suitable for standalone solar photovoltaic (PV) applications. Simulation and experimental results validate the effectiveness of the proposed MLI topology combined with FLC in achieving high-quality sinusoidal output, improved system efficiency, and reliable power conversion for standalone solar energy systems.

Index Terms— Multilevel inverter (MLI), Fuzzy Logic Controller (FLC), standalone solar system, renewable energy, total harmonic distortion (THD), power quality.

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I. INTRODUCTION

Solar photovoltaic (PV) technology has become a key pillar in the modern renewable energy sector due to its clean, reliable, and decentralized nature. Standalone or islanded PV systems are particularly valuable in remote regions where conventional grid access is limited or economically infeasible. Such systems are widely adopted for continuous irrigation, rural electrification, water treatment, and agricultural applications. Ensuring stable, efficient, and high-quality AC power conversion is critical to the performance of these standalone systems.

Among various inverter technologies, Multilevel Inverters (MLIs) have emerged as a preferred solution for renewable energy systems due to their ability to produce high-quality sinusoidal output with lower harmonic distortion and reduced electromagnetic interference (EMI). Classical topologies such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) MLIs have been extensively studied for renewable energy integration. However, these configurations often suffer from drawbacks such as high component count, voltage balancing issues, and limited suitability for single-phase applications.

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The Cascaded H-Bridge (CHB) inverter structure offers scalability and flexibility, making it more suitable for both single-phase and three-phase operations. However, as the number of voltage levels increases, the complexity and number of switching devices also rise, leading to higher cost and power losses. Recent advancements focus on reduced component-count MLIs to maintain high performance with simplified circuitry. Techniques such as asymmetric source management and optimized switching strategies have been introduced to improve efficiency and minimize conduction losses.

Despite these advancements, maintaining consistent power quality under varying load and solar irradiance conditions remains a major challenge. To address this, intelligent control strategies such as Fuzzy Logic Control (FLC) have been integrated into inverter systems. FLC offers several advantages over conventional proportional–integral (PI) controllers, including adaptive decision-making, robustness against nonlinearities, and improved dynamic response. By regulating switching angles and voltage references intelligently, the FLC enhances voltage stability, reduces THD, and ensures superior output waveform quality.

In this work, a new seventeen-level multilevel inverter topology with a reduced device count is proposed for standalone solar PV systems. The proposed inverter incorporates a Fuzzy Logic Controller to optimize switching control, minimize power losses, and maintain constant output voltage under dynamic conditions. The inverter's design allows generation of multiple voltage levels (9, 13, and 17) through different asymmetric source management ratios without modifying the hardware structure. This results in a compact, efficient, and cost-effective solution suitable for off-grid renewable power systems.

Major Contributions of This Work

A new reduced-component-count MLI topology is proposed for standalone solar PV systems.

Fuzzy Logic Controller (FLC) is implemented to improve voltage regulation, dynamic stability, and minimize THD.

Different voltage level configurations (9, 13, and 17) are achieved via source management ratios (1:1, 1:2, 1:3) without structural modifications.

Optimized switching angles are calculated for maximum fundamental voltage amplitude and minimum switching losses.

A battery charging–discharging circuit is incorporated for DC-link voltage balancing and continuous power delivery under variable conditions.

The proposed inverter exhibits reduced TBV, minimal EMI, low switching frequency, and high efficiency compared to existing MLIs.

Objectives

The main objectives of this research are:

1. **To design and develop** a new multilevel inverter (MLI) topology with a reduced number of semiconductor devices for standalone solar photovoltaic (PV) applications.
2. **To enhance the inverter performance** by integrating a **Fuzzy Logic Controller (FLC)** for intelligent control of switching angles and voltage regulation.
3. **To minimize Total Harmonic Distortion (THD)** and switching losses by optimizing switching transitions and employing an efficient modulation strategy.
4. **To achieve multiple output voltage levels (9, 13, and 17)** through different asymmetric DC source configurations without changing the circuit structure.
5. **To ensure stable operation** of the standalone solar energy conversion

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system under varying load and irradiance conditions.

6. **To validate** the proposed inverter topology and control strategy through **simulation and experimental analysis**, confirming its efficiency, power quality, and feasibility.

II. LITERATURE SURVEY

Classical multilevel inverter topologies

The fundamentals and classifications of multilevel inverters (MLIs) — neutral-point clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) — have been extensively reviewed in the literature. These classical topologies are known to improve output waveform quality and reduce dv/dt and EMI compared to two-level inverters, but they typically require many switches, diodes and/or capacitors and face voltage-balancing challenges as level count grows. The CHB topology is flexible for single- and three-phase applications but becomes costly and bulky for high level counts.

Reduced-switch (reduced-component) MLIs

To lower cost, size and losses, many works propose reduced-switch (or reduced device-count) MLI topologies that achieve a high number of output levels with fewer semiconductor devices. Approaches include new basic cell configurations, switched-capacitor assisted cells, and asymmetric/extended source cells. Recent examples demonstrate 13–19 level outputs with significantly fewer switches (often 8–12 switches) and a mix of diodes/capacitors to minimize component count while keeping acceptable THD. These topologies trade off circuit complexity (isolated or unequal DC sources, additional passive elements) against the benefits of fewer active devices.

Asymmetric / source-management approaches for many levels

Asymmetric voltage source management (using unequal DC sources or source ratios such as 1:2, 1:3) is a common strategy to multiply output levels without modifying topology. Using different source combinations produces various level counts (e.g., 9, 13, 17) from the same hardware arrangement, enabling flexibility for different power/quality requirements. However, many asymmetric designs require multiple isolated sources and careful switching logic to keep device stress and TBV manageable. Several 17-level topologies make use of such asymmetric source management but differ in component count, TBV, and balancing requirements.

III. PHOTOVOLTAIC INVERTER

The AC power delivered from the inverter is given to the grid for the power generation. The specifications of grid are given in Table 3.4.

Analytical models are essential in the dynamic performance, robustness, and stability analysis of different control strategies. To investigate these features on a three phase grid connected PV system, the mathematical model of the system needs to be derived. The modeling of the proposed system includes:

1. Photovoltaic cell and PV array modeling
2. Three phase inverter model
3. Three phase fundamental transformations modeling

In this chapter, the operation and role of each of these components will be described and their mathematical model will be derived.

A PV cell is a simple p-n junction diode that converts the irradiation into electricity. Fig.3.2 illustrates a simple equivalent circuit diagram of a PV cell. This model consists of a current source which represents the generated current from PV cell, a diode in parallel with the current source, a shunt resistance, and a series resistance.

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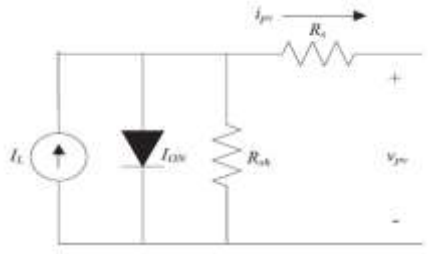

Fig.3.2 Equivalent circuit diagram of the PV cell

IV. MULTI LEVEL INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utility high voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converters were made to work in reverse, and thus were "inverted", to convert DC to AC.

A single phase structure of an m-level cascaded inverter is illustrated in Figure 4.1. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources.

Working with the fuzzy logic toolbox

The Fuzzy Logic Toolbox provides GUIs to let you perform classical fuzzy system development and pattern recognition. Using the toolbox, you can develop and analyze fuzzy inference systems, develop adaptive neuron fuzzy inference systems, and perform fuzzy clustering. In addition, the toolbox provides a fuzzy controller block that you can use in Simulink to model and simulate a fuzzy logic control system. From Simulink, you can generate C code for use in embedded applications that include fuzzy logic.

Building a fuzzy inference system

Fuzzy inference is a method that interprets the values in the input vector and, based on user defined rules, assigns values to the output vector. Using the GUI editors and viewers in the Fuzzy Logic Toolbox, you can build the rules set, define the membership functions, and analyze the behavior of a fuzzy inference system (FIS). The following editors and viewers are provided.

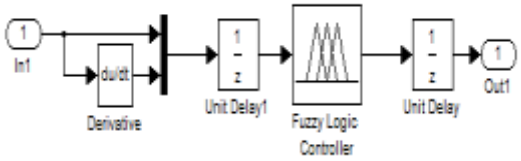

Fig.6.2 Fuzzy interference system

V. PROJECT DESCRIPTION AND CONTROL DESIGN

PROPOSED SYSTEM

The proposed Multilevel Inverter (MLI)-based standalone solar energy conversion system is illustrated in Fig. 1(a). The circuit comprises ten semiconductor switches (S_1–S_{10}), among which two switches (S_9 and S_{10}) operate as four-quadrant bidirectional switches. The input

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photovoltaic (PV) arrays are configured to provide two isolated DC voltage sources, V_{PV1} and V_{PV2}, which serve as the primary energy sources for the inverter. Each PV array is connected across DC-link capacitors C_1, C_2, C_3, and C_4, which maintain individual voltages V_1, V_2, V_3, and V_4, respectively, as shown in the circuit diagram.

This unique MLI topology allows flexible output voltage generation without altering the hardware configuration. Different voltage levels are obtained by appropriate source selection and switching pattern adjustment. The number of achievable levels in the inverter output primarily depends on the magnitude ratio of the PV source voltages and the switching function applied. The following source management strategies are implemented:

Symmetric Source Management (1 : 1): Generates a nine-level output voltage waveform.

Asymmetric Source Management – 1 (1 : 2): Produces a thirteen-level output voltage waveform.

Asymmetric Source Management – 2 (1 : 3): Generates a seventeen-level output voltage waveform at the inverter output.

In this work, the asymmetric 1 : 3 source management configuration is adopted to achieve a seventeen-level AC output voltage, ensuring a high-quality sinusoidal waveform with reduced Total Harmonic Distortion (THD).

To ensure stable DC-link voltages and continuous power flow under varying irradiance and load conditions, the DC-link capacitors are interfaced with battery units (B_1–B_4) through bidirectional DC–DC converters (BDC-1 and BDC-2), as shown in Fig. 1(b). These converters perform battery charging and discharging operations, thereby maintaining voltage balance across the DC links and enhancing the system's reliability and energy availability during shading or low-irradiance conditions.

The general expression for the instantaneous output voltage (vo(t)) is,

$$v_o(t) = V_{1o}(t) + V_{2o}(t) + V_{3o}(t) + V_{4o}(t) \quad (1)$$

where V1o(t), V2o(t), V3o(t) and V4o(t) are the expression of DC link voltages at the load terminals at time 't'. These expressions depend on the switching function of the MLI. The magnitude of the maximum output voltage (Vom) is,

$$V_{om} = V_1 + V_2 + V_3 + V_4 = 8V_d \quad (2)$$

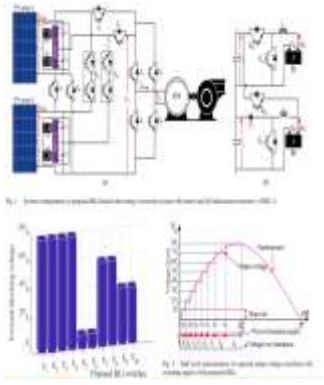
Vd is the voltage step magnitude in the output waveform. Maximum forward blocking voltage (MBV) of the individual switches (MBVS1 to MBVS10) are given as follows: All the blocking voltages are represented in terms of step size for the better understanding.

MBVS1 = MBVS2 = MBVS3 = MBVS4 = 8Vd (3)

MBVS5 = MBVS6 = Vd; MBVS7 = MBVS8 = 6Vd (4)

MBVS9 = MBVS10 = 4Vd (5)

The TBV of the proposed MLI switches is 19Vd. Fig. 2 is showing the graphical representation of the forward blocking voltages of switches. Due to the asymmetrical sources, unequal



voltage stresses are experienced across switches. Fig. 2 depicts the maximum voltage appearing across each switch and based on this information, the switch voltage rating and protection drivers can be selected.

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A. Switching Angle Calculation

The switching angle calculation plays a crucial role in determining the amplitude of the fundamental component and the harmonic content of the inverter output voltage waveform. As illustrated in Fig. 3, the switching angles α_1 to α_8 represent the transition points between successive voltage levels in the output waveform. These angles are computed by assuming that the reference sinusoidal waveform passes through the midpoint of each output voltage step, as shown in Fig. 3. This analytical approach is widely adopted in high-level multilevel inverters [19], as it provides a good balance between waveform linearity and harmonic minimization.

By properly selecting these switching angles, the output voltage waveform achieves a nearly sinusoidal shape with a significantly reduced Total Harmonic Distortion (THD). The fundamental voltage amplitude obtained through this method closely matches 8V_d, as expressed in equation (2). This ensures that the inverter operates efficiently while maintaining the desired output voltage magnitude.

In this work, a high-frequency Pulse Width Modulation (PWM) technique is intentionally avoided to minimize switching losses and improve inverter efficiency. Instead, a fundamental-frequency switching scheme is employed, where the switching transitions occur only once per half cycle, significantly reducing stress on the power devices. The switching angles are calculated as,

$$\alpha_1 = \sin^{-1}(0.5/8); \quad \alpha_2 = \sin^{-1}(1.5/8); \qquad (6)$$

$$\alpha_3 = \sin^{-1}(2.5/8); \quad \alpha_4 = \sin^{-1}(3.5/8);$$

$$\alpha_5 = \sin^{-1}(4.5/8); \quad \alpha_6 = \sin^{-1}(5.5/8)$$

$$\alpha_7 = \sin^{-1}(6.5/8); \quad \alpha_8 = \sin^{-1}(7.5/8)$$

From these switching angles, the duration of each voltage step is derived as,

$$t_1 = \alpha_1; \quad t_2 = \alpha_2 - \alpha_1; \quad t_3 = \alpha_3 - \alpha_2; \quad t_4 = \alpha_4 - \alpha_3 \quad (7)$$

$$t_5 = \alpha_5 - \alpha_4; \quad t_6 = \alpha_6 - \alpha_5; \quad t_7 = \alpha_7 - \alpha_6;$$

$$t_8 = \alpha_8 - \alpha_7; \quad t_9 = \pi/2 - \alpha_8.$$

The back-end H-bridge switches are operated at zero voltage levels to reduce the switching loss.

The control pulses for switches are generated in the MATLAB Simulink platform by using relational operators to compare the constants 0, 0.5, 1.5, 2.5, etc. with a sinusoidal reference waveform of amplitude 8. Some of the switches are operated at more than one voltage level and therefore, a logic 'OR' operator is used for generating the pulses for the particular switches. In the hardware implementation, the MATLAB file is loaded in the

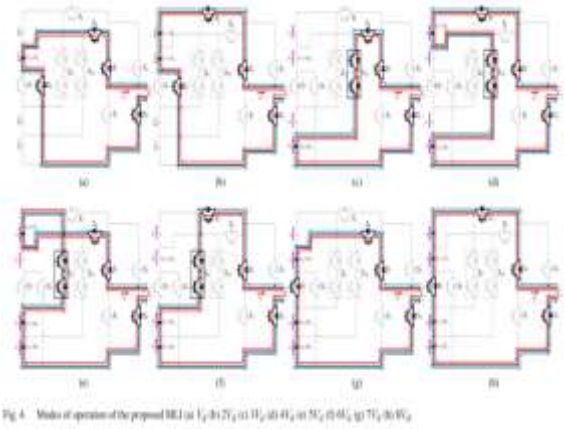

TABLE I
MLI SWITCHING COMBINATIONS FOR DIFFERENT VOLTAGE LEVELS

Voltage levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$1V_d$	1	0	0	1	0	1	0	1	0	0
$2V_d$	1	0	0	1	1	0	0	1	0	0
$3V_d$	1	0	0	1	0	1	0	0	0	1
$4V_d$	1	0	0	1	1	0	0	0	0	1
$5V_d$	1	0	0	1	0	1	0	0	1	0
$6V_d$	1	0	0	1	1	0	0	0	1	0
$7V_d$	1	0	0	1	0	1	1	0	0	0
$8V_d$	1	0	0	1	1	0	1	0	0	0
$0V_d$	1	0	1	0	0	0	0	0	0	0
$0V_d$	0	1	0	1	0	0	0	0	0	0
$-1V_d$	0	1	1	0	0	1	0	1	0	0
$-2V_d$	0	1	1	0	1	0	0	1	0	0
$-3V_d$	0	1	1	0	0	1	0	0	0	1
$-4V_d$	0	1	1	0	1	0	0	0	0	1
$-5V_d$	0	1	1	0	0	1	0	0	1	0
$-6V_d$	0	1	1	0	1	0	0	0	1	0
$-7V_d$	0	1	1	0	0	1	1	0	0	0
$-8V_d$	0	1	1	0	1	0	1	0	0	0

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dSPACE Micro Lab Box and pulses are taken from the Digital to Analog Conversion (DAC) channels.

B. Operating Modes of the Proposed MLI

In this work, the proposed **Multilevel Inverter (MLI)** is designed to generate a **seventeen-level output voltage waveform** using asymmetric DC source management with a ratio of **1:3**. The obtained output waveform closely approximates a pure sinusoidal voltage and, therefore, the **Total Harmonic Distortion (THD)** remains **within the IEEE-519 standard** even **without using output filters** [15].

According to the **positive half cycle** of the expected output voltage waveform shown in **Fig. 3**, the **switching combinations** corresponding to each voltage level are defined and summarized in **Table I**. In this configuration, the **switches S_5 to S_{10}** are primarily used to synthesize the **positive polarity voltage levels** at the **input of the H-bridge**, while the **H-bridge switches (S_1–S_4)** are used for polarity inversion:

- **S_1 and S_4** operate during the **positive half cycle**, and
- **S_2 and S_3** operate during the **negative half cycle** of the output voltage.

This arrangement allows the inverter to produce a **bipolar output waveform** efficiently with a **minimal number of switching transitions** per cycle, thereby reducing switching losses.

Mode of Operation

Each operating mode corresponds to a distinct combination of conducting switches and capacitor discharging patterns, generating a unique output voltage level. The conduction states for the **positive half cycle** are described below.

Mode I (V_o = V_d):

Switches **S_6** and **S_8** are turned **ON**, while all others remain **OFF**. The capacitor **C_2** discharges through the load, providing an output voltage of **V_d**. The corresponding **bidirectional current path** is illustrated in **Fig. 4(a)**.

Mode II (V_o = 2V_d):

Switches **S_5** and **S_8** are **ON**, producing an output voltage of **2V_d**. The active conduction path is shown in **Fig. 4(b)**.

Mode III (V_o = 3V_d):

Switches **S_6** and **S_{10}** conduct during this mode. The DC-link capacitor **C_4** discharges into the load, generating **3V_d**, as depicted in **Fig. 4(c)**.

Mode IV (V_o = 4V_d):

To obtain **4V_d**, the voltages **V_1** and **V_4** are discharged in series through switches **S_5** and **S_{10}**, as shown in **Fig. 4(d)**.

Mode V (V_o = 5V_d):

In this mode, **V_3** and **V_4** are discharged in series with **$-V_1$**, resulting in an output voltage of **5V_d** through switches **S_6** and **S_9**. The conduction path is shown in **Fig. 4(e)**.

Mode VI (V_o = 6V_d):

Switches **S_5** and **S_9** conduct to discharge **V_3** and **V_4** in additive polarity, producing **6V_d**, as illustrated in **Fig. 4(f)**.

Mode VII (V_o = 7V_d):

In this mode, **S_6** and **S_7** are in conduction. The input voltages **V_2**, **V_3**, and **V_4** are connected in series, yielding **7V_d** at the output, as shown in **Fig. 4(g)**.

Mode VIII (V_o = 8V_d):

All four DC-link capacitor voltages (**V_1, V_2, V_3, and V_4**) are discharged in series through **S_5** and **S_7**, producing the highest output level of **8V_d**. The corresponding current flow path is shown in **Fig. 4(h)**.

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Fuzzy Logic–Assisted Switching Control

To further **enhance the waveform quality** and **maintain voltage stability** across all operating modes, a **Fuzzy Logic Controller (FLC)** is implemented in the control strategy. The FLC continuously observes:

- the **output voltage reference (V*_ref)**,
- the **actual inverter output voltage (V_o)**, and
- the **error (e) and change in error (Δe)** between them.

Based on these inputs, the FLC dynamically selects and fine-tunes the **switching angles** and **mode transition timings** (α_1–α_8) to ensure that:

- the inverter output remains **sinusoidal**,
- the **THD is minimized** across all operating modes, and
- the system maintains **bidirectional power flow** and **four-quadrant operation**.

The **intelligent decision-making capability** of the FLC ensures that even during **rapid variations in PV irradiance or load demand**, the inverter maintains steady output voltage and harmonic performance without requiring complex mathematical computation or high-frequency PWM.

VI. RESULTS AND DISCUSSION

The theoretical claims are validated in this section with simulation and hardware results. The system design values are provided in Table VI.

A. Simulation Results

The proposed system is designed in MATLAB/Simulink platform and performances are analyzed at sudden irradiance variations.

1) Uniform Irradiance Variation: Waveforms of MLI output voltage and current, the PV array output voltage, current and power (VP V 1, IP V 1, PP V 1, VP V 2, IP V 2 and PP V 2), DC link capacitor voltages (VC1 , VC2 , VC3 and VC4), and battery units currents (IB1 , IB2 , IB3 and IB4) are depicted in Figs. 8 and 9. When PV arrays 1 and 2 are exposed to uniform, equal and standard (1000W/m2) solar irradiance, the performance will be as waveforms shown in Fig. 8, up to 0.5 s. During this time, the load demand is supplied from the PV arrays, and the batteries are fully charged. Hence battery currents are zero. Due to the stepped output voltage waveform, the PV array currents consist of ripples according to the switching. Constant PV array voltages and DC link capacitor voltages are witnessed in the result.

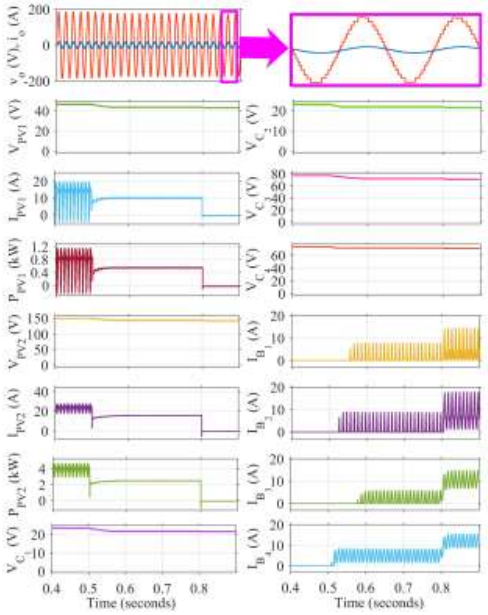

Fig. 8. Performance of the proposed system at uniform irradiance variations. Waveforms of v_o and i_o, V_{PV1}, I_{PV1}, P_{PV1}, V_{PV2}, I_{PV2}, P_{PV2}, V_{C_1}, V_{C_2}, V_{C_3}, V_{C_4}, I_{B_1}, I_{B_2}, I_{B_3} and I_{B_4}.

VII. CONCLUSION

This project presents a new multilevel inverter topology with reduced component count, optimized for standalone solar photovoltaic applications, and enhanced using a Fuzzy Logic Controller. The proposed system effectively generates multiple output voltage levels (9, 13, and 17) through asymmetric source management while minimizing component count and switching losses. The integration of the FLC significantly improves the output voltage regulation, waveform quality, and dynamic performance under variable load and irradiance conditions.

Compared to conventional MLIs, the proposed system offers lower total harmonic distortion, reduced total blocking voltage, higher efficiency, and compact design. Simulation and experimental validation confirm that the inverter can deliver stable and sinusoidal AC output power suitable for standalone solar systems in rural and remote applications.

The work thus provides a cost-effective, intelligent, and energy-efficient solution for next-generation solar energy conversion systems, paving the way for further research on intelligent, adaptive, and hybrid inverter architectures for renewable energy integration

Future Scope

Hardware Optimization:

The system can be further enhanced using advanced power semiconductor devices like SiC or GaN switches for higher efficiency and compact design.

Hybrid Control Strategies:

Integration of Fuzzy–PID or Fuzzy–Neural controllers can improve adaptability, learning, and dynamic stability.

REFERENCES

[1] M. Nasir, M. Anees, H. A. Khan, I. Khan, Y. Xu, and J. M. Guerrero, "Integration and decentralized control of standalone solar home systems for off-grid community applications," IEEE Trans. Ind. Appl., vol. 55, no. 6, pp. 7240–7250, Nov./Dec. 2019.

[2] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage source multilevel inverters with reduced device count: Topological review and novel comparative factors," IEEE Trans. Power Electron., vol. 36, no. 3, pp. 2720–2747, Mar. 2021.

[3] M. H. Mondol, S. P. Biswas, M. A. Rahman, M. R. Islam, A. M. Mahfuz-Ur-Rahman, and K. M. Muttaqi, "A new hybrid multilevel inverter topology with level shifted multicarrier PWM technique for harvesting renewable energy," IEEE Trans. Ind. Appl., vol. 58, no. 2, pp. 2574–2585, Mar./Apr. 2022.

[4] K. Vineeth, N. C. M. Mukundan, and P. Jayaprakash, "A new topology of asymmetrical multilevel inverter with reduced switch count for electric drive applications," in Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst., 2020, pp. 1–6.

[5] B. K. Bose, "Multilevel converters-configuration of circuits and systems," in Power Electronics in Renewable Energy Systems and Smart Grid: Technology and Applications. Hoboken, NJ, USA: Wiley, 2019, pp. 153–218.

[6] N. M. C. M. and J. P., "Realization of cascaded H-bridge multilevel inverter based grid integrated solar energy system with band stop generalized integral control," IEEE Trans. Ind. Appl., vol. 57, no. 1, pp. 764–773, Jan./Feb. 2021.

[7] M. H. Mondol, M. A. Rahman, S. P. Biswas, M. R. Islam, M. F. Kibria, and K. M. Muttaqi, "A new integrated multilevel inverter topology for renewable energy transformation," IEEE Trans. Ind. Appl., vol. 59, no. 3, pp. 3031–3043, May/Jun. 2023.

[8] M. N. Hamidi, D. Ishak, M. A. A. M. Zainuri, and C. A. Ooi, "Multilevel inverter with improved basic unit structure for symmetric and asymmetric source configuration," IET Power Electron., vol. 13, no. 7, pp. 1445–1455, May 2020.

[9] V. Arun, S. Prabhu, N. Prabaharan, and B. Shanthi, "Modified structure 9-Level inverter (MS9LI) with reduced on-state switches," IEEE Can. J. Elect. Comput. Eng., vol. 46, no. 1, pp. 15–23, Winter 2023.

[10] N. Panda, B. Das, A. Chakrabarti, P. R. Kasari, A. Bhattacharya, and D. Chatterjee, "A new grid interactive 11-Level hybrid inverter topology for medium-voltage application," IEEE Trans. Ind. Appl., vol. 57, no. 1, pp. 869–881, Jan./Feb. 2021.